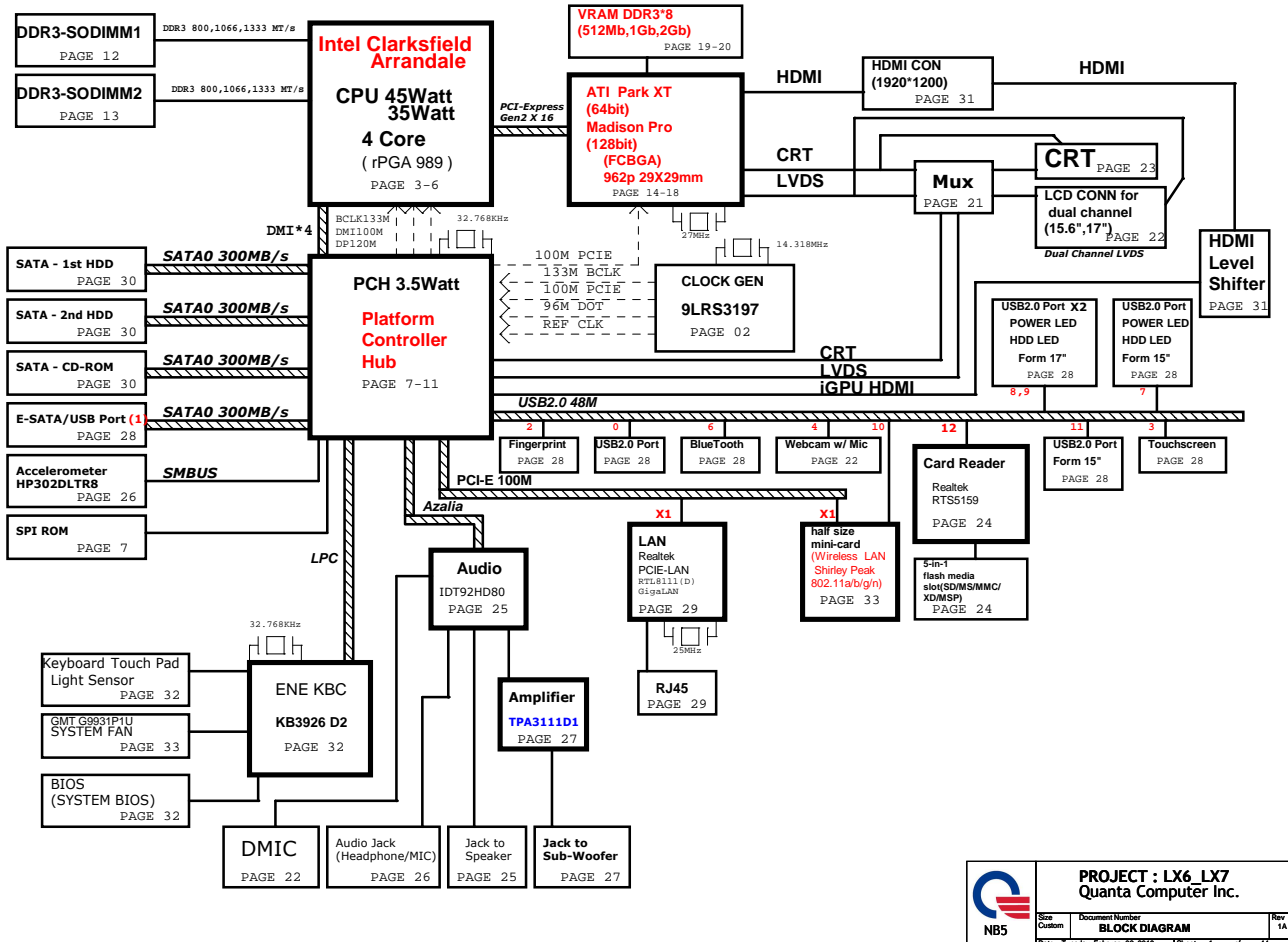
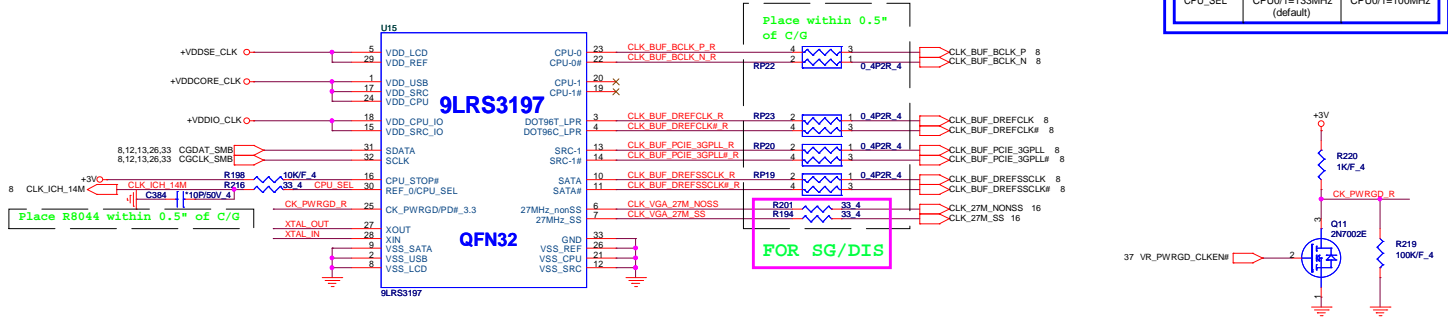
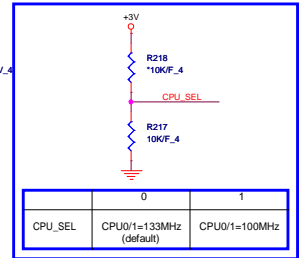
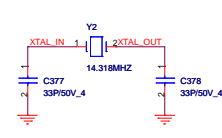
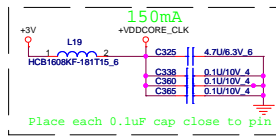
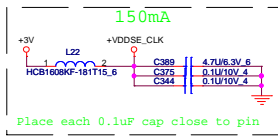
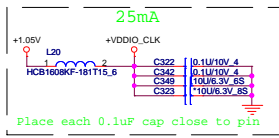


LX6/7 (Liverpool) BLOCK DIAGRAM

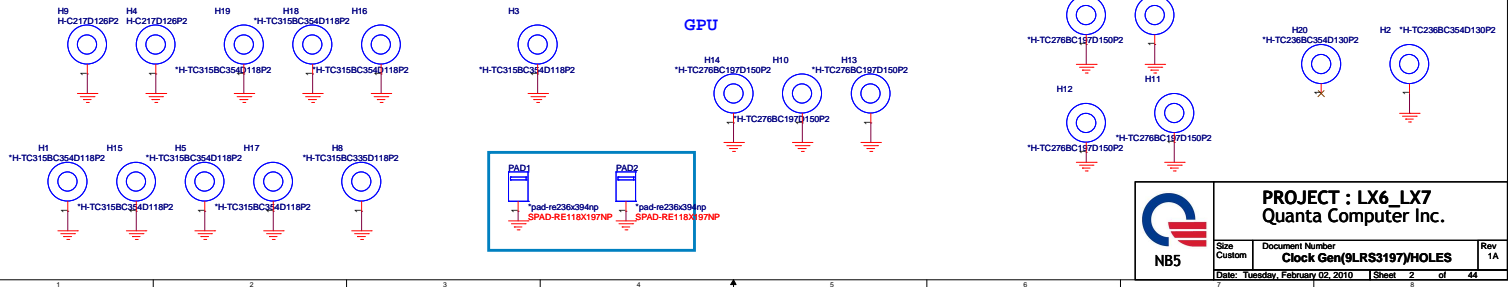
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



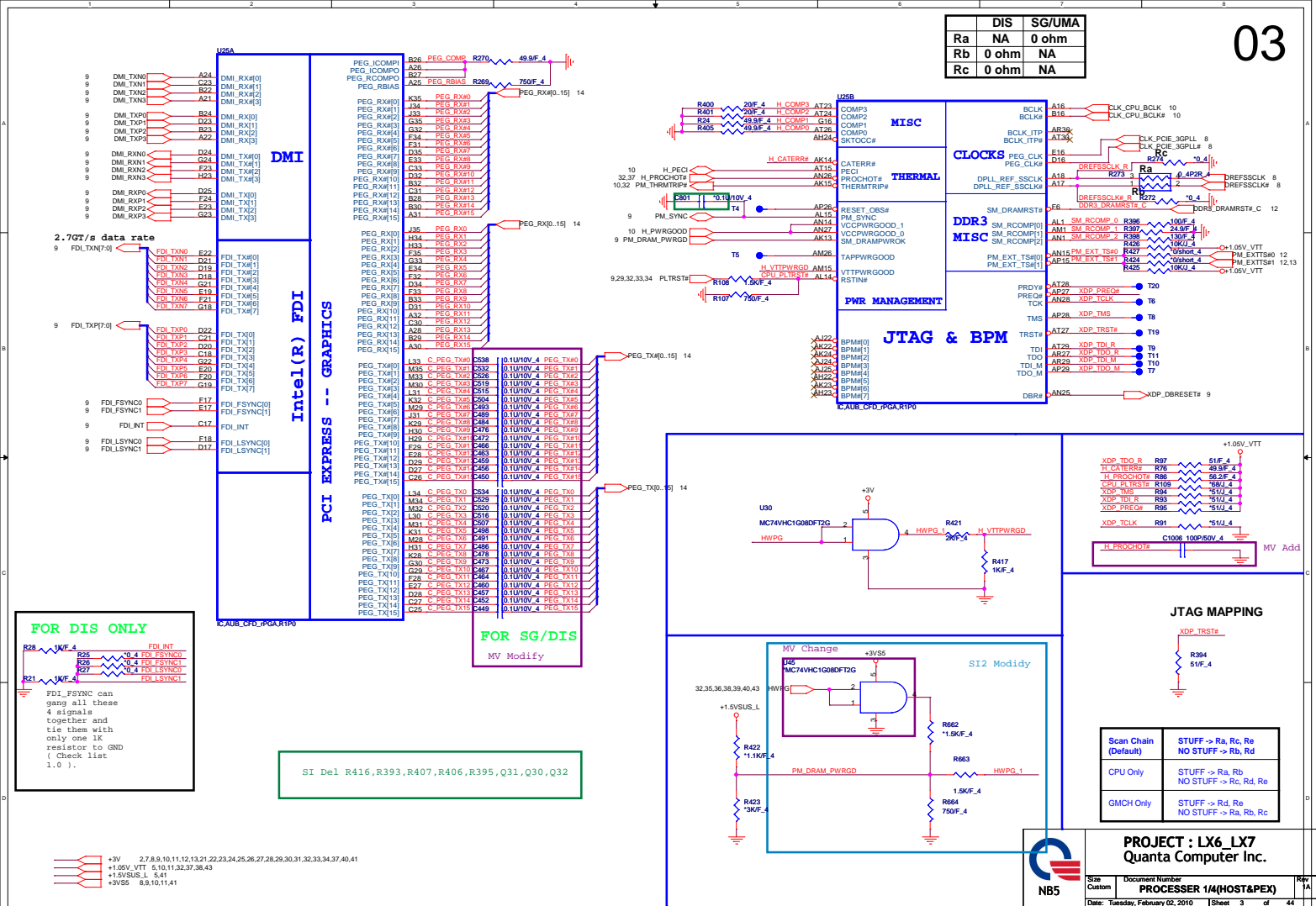


+1.05V 7,8,9,11,36,37,43
 +1.5V 33,41
 +3V 3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41

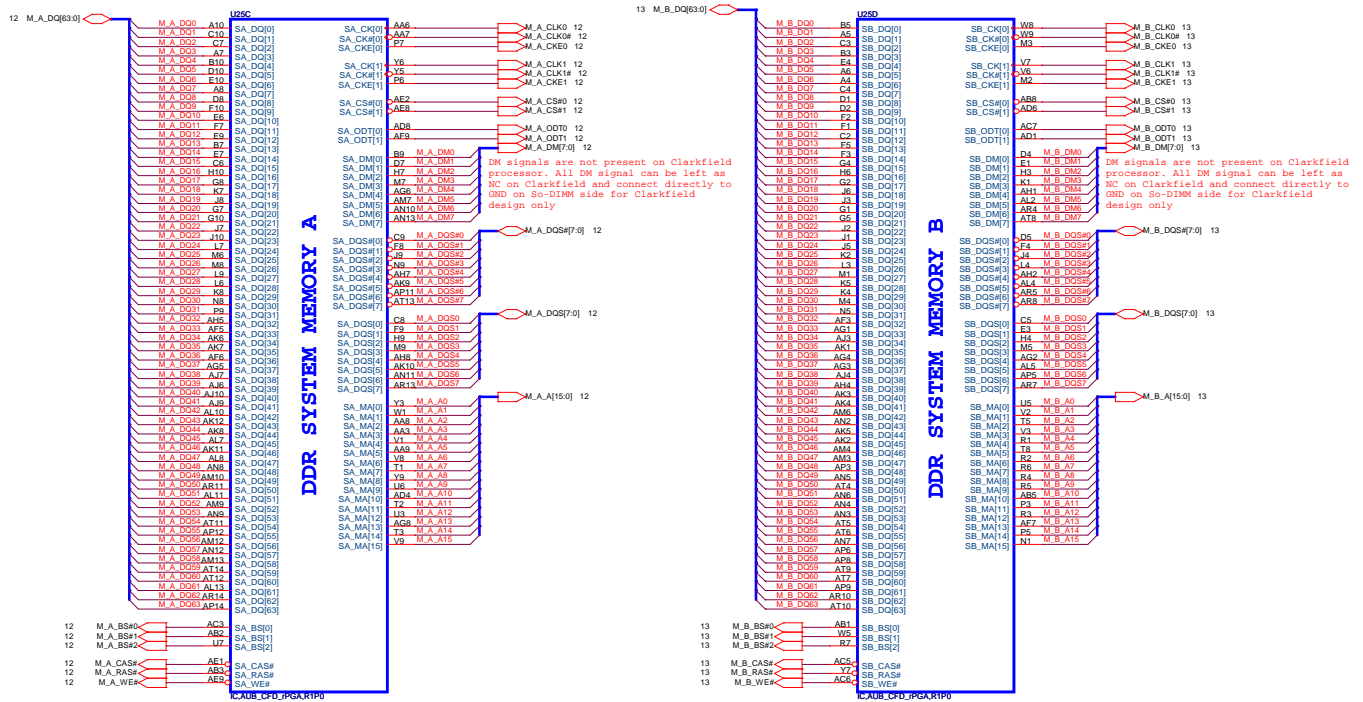
HOLE

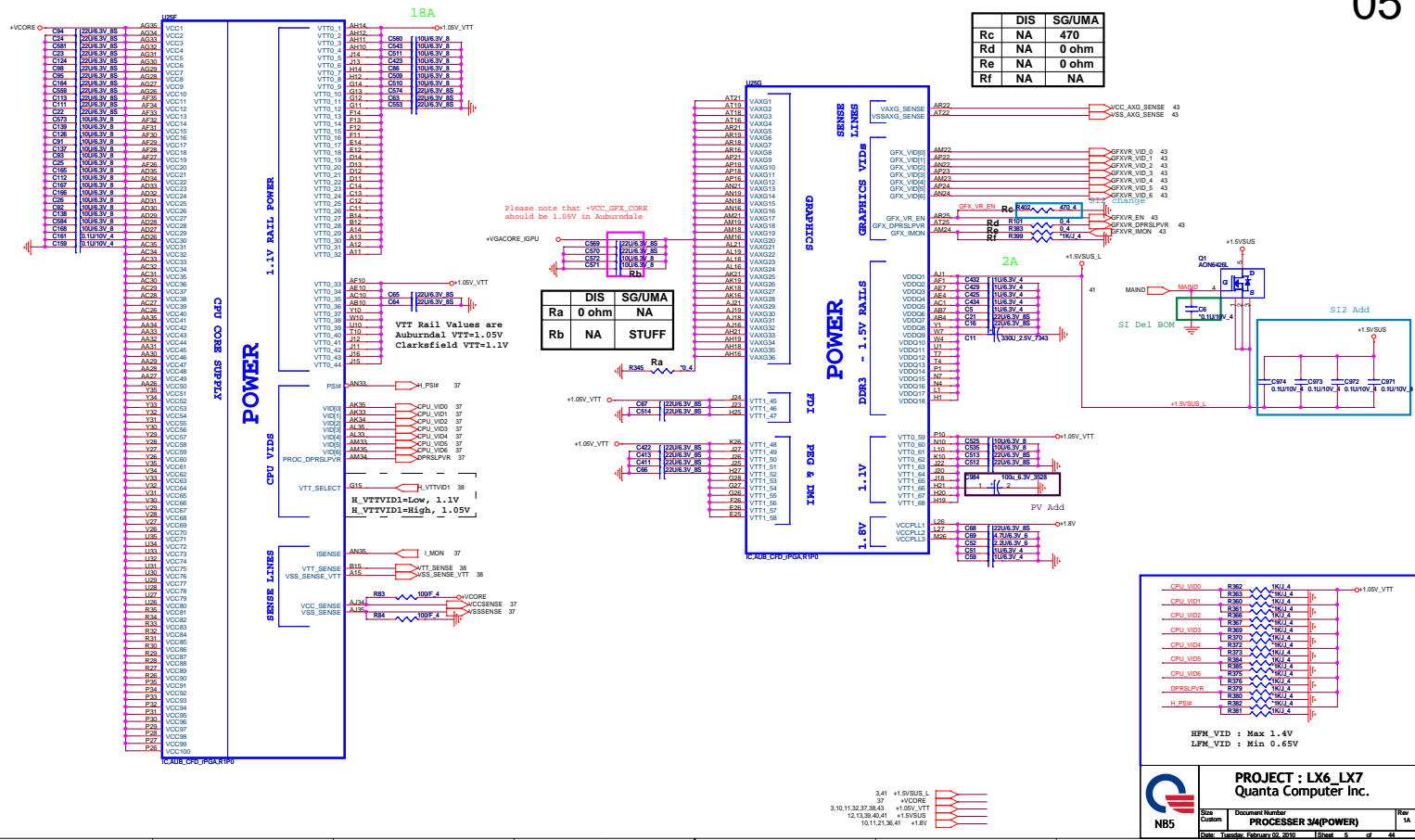


	DIS	SG/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

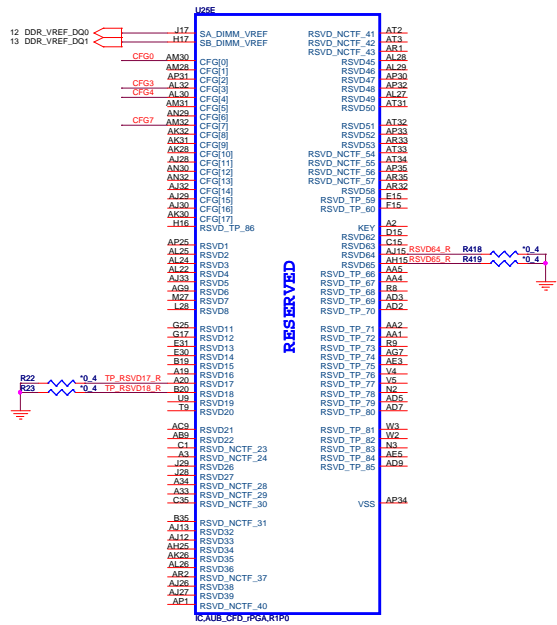
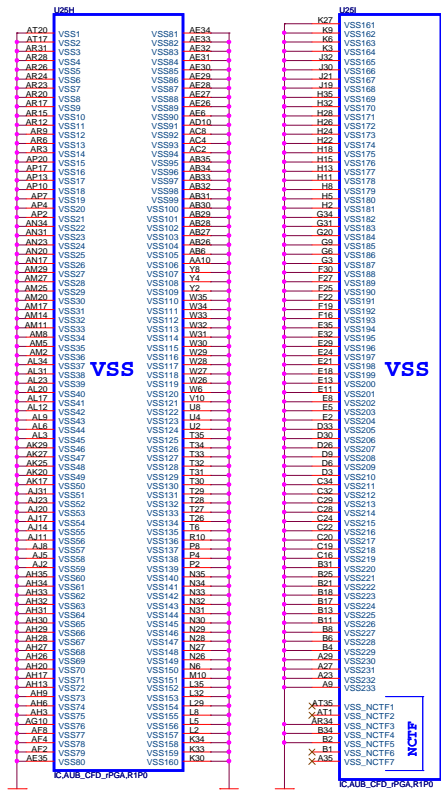




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

06



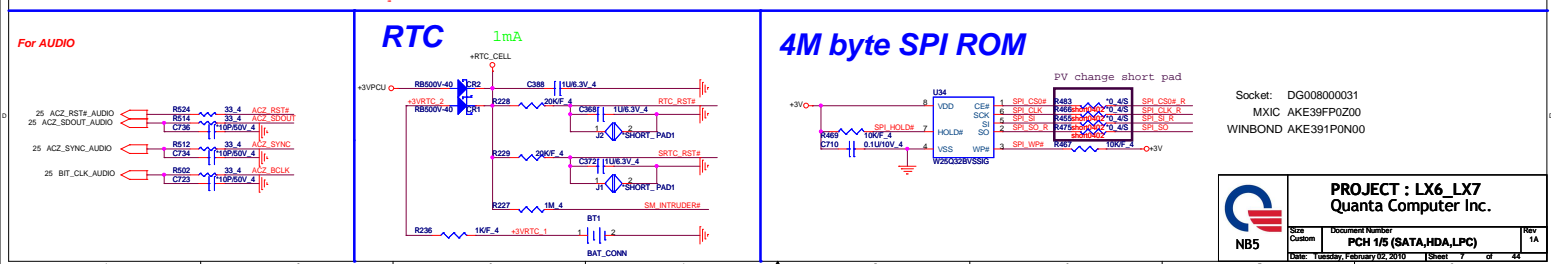
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0, 14 -> 1

	UMA	SG/DIS
R90	NA	NA
R77	NA	3.01K
R79	NA	NA
R87	NA	NA

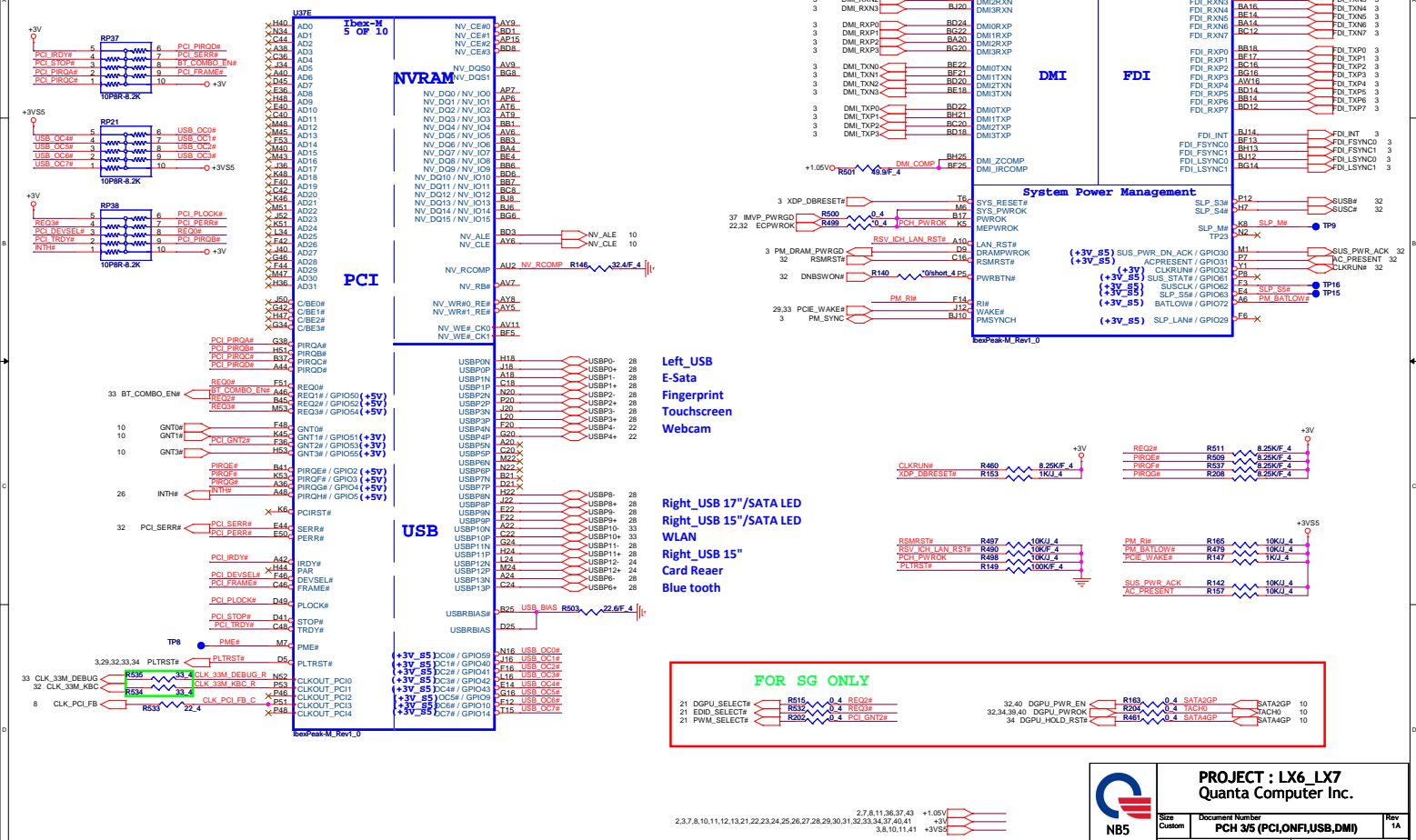
CFG[1:0] - PCI_Epress Configuration Select	
* 11= 1 x 16 PEG	
* 10= 2 x 8 PEG	

NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	Rev 1A
Size Custom	Document Number PROCESSOR 44 (GND)	Date: Tuesday, February 02, 2010 Sheet 6 of 44





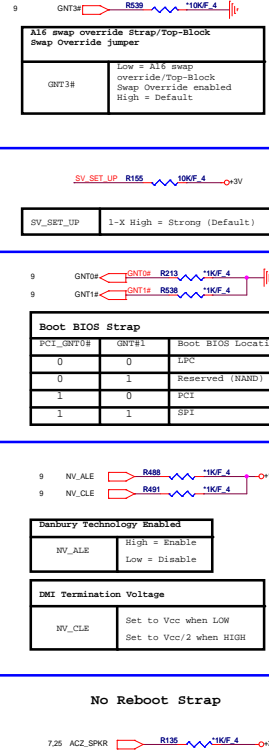
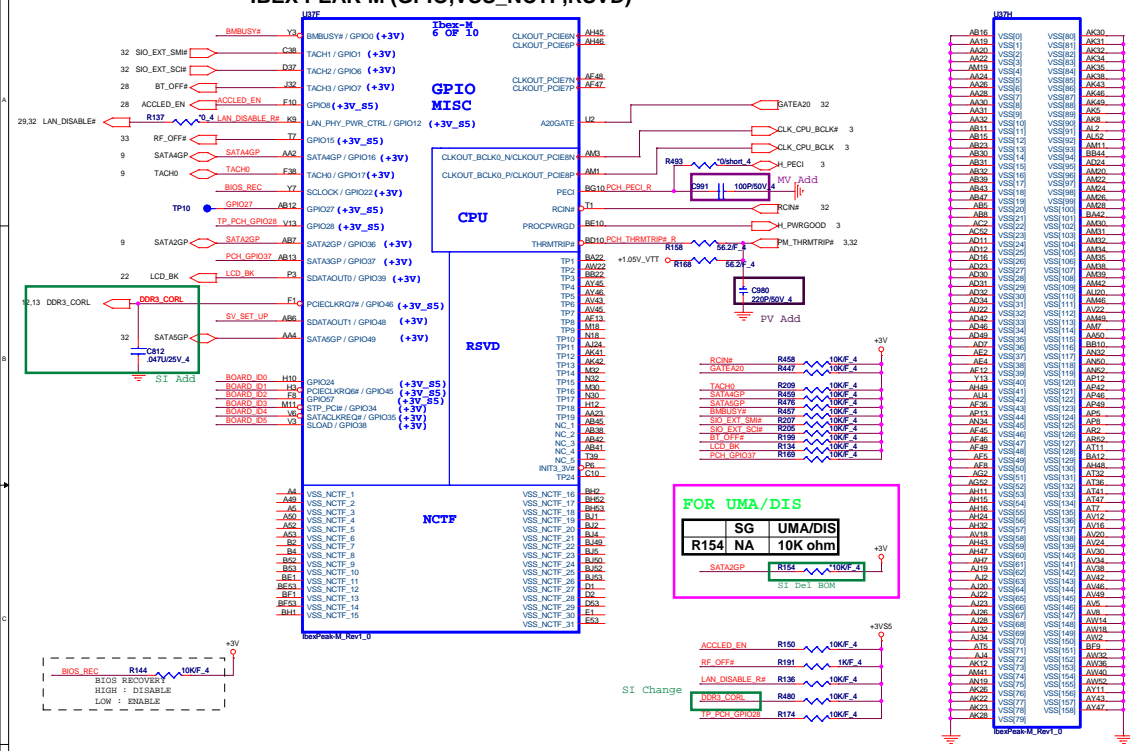
IBEX PEAK-M (PCI, USB, NVRAM)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

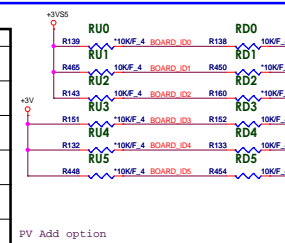
10



BOARD ID SETTING

Board ID	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RD0 (1)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LX6	0	1				
LX7	1	0				
Discrete			0	0		
UMA			0	1		
SG			1	0		
LX7_No Subwoofer	1	1				



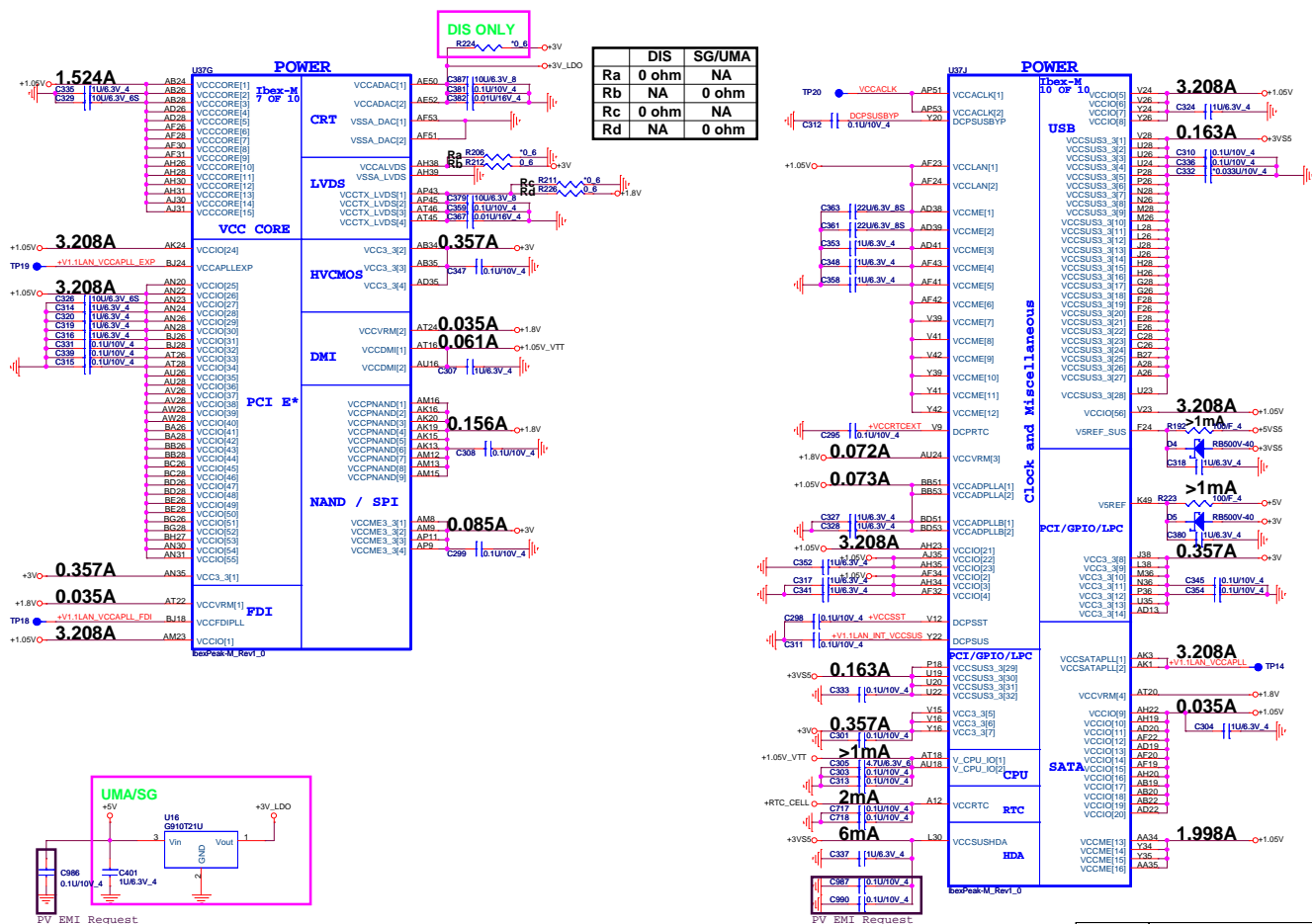
+3V 2.17,8.5,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41

+1.8V 5,11,21,36,41

+3V5 3,8,9,11,41

+1.05V_VTT 3,5,11,32,37,38,43

NB5	PROJECT : LX6_LX7	
	Quanta Computer Inc.	
Rev	Docu	Rev
1A	1A	1A
Date	Monday, February 13, 2010	Sheet 10 of 44



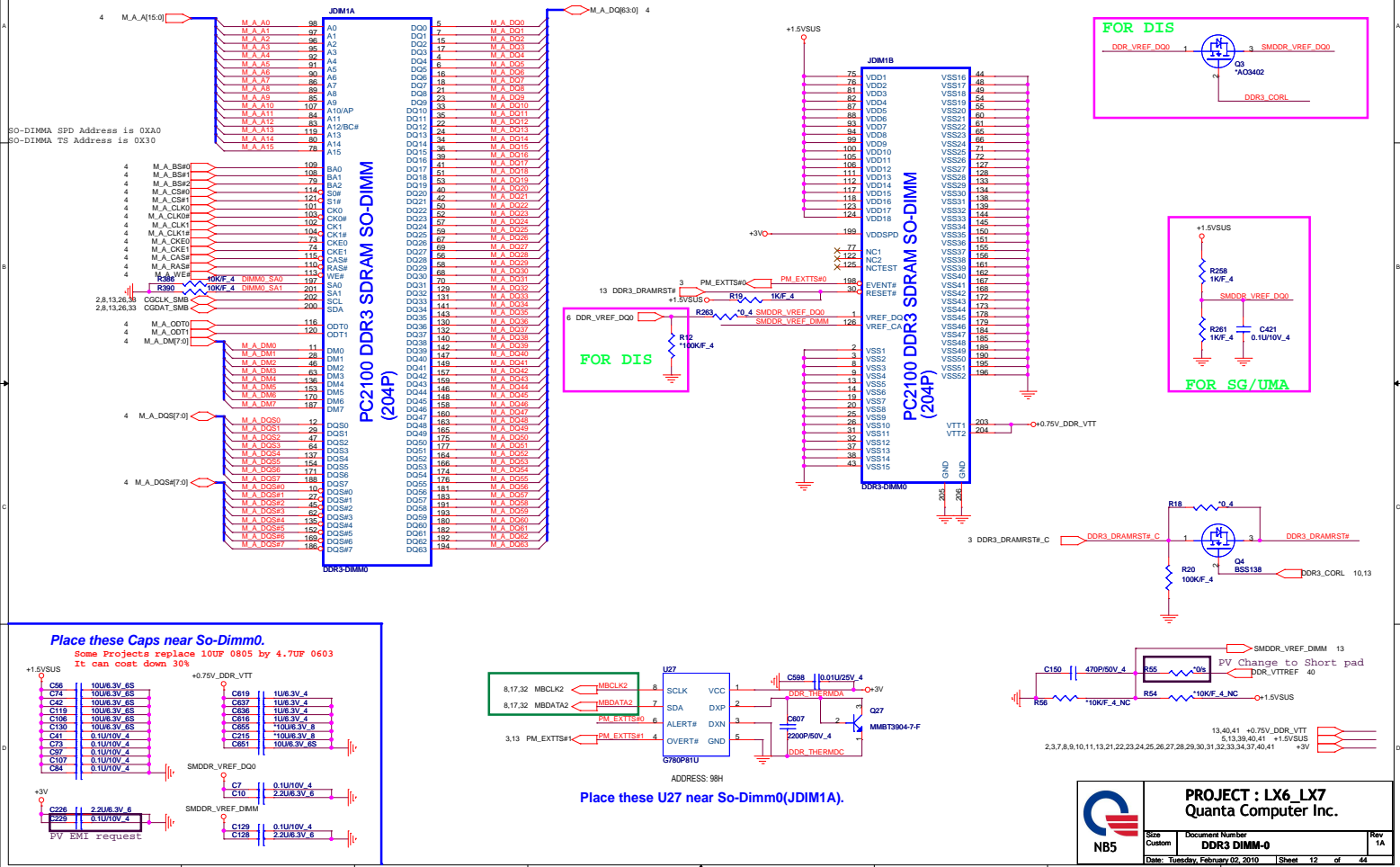
	DIS	SG/UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

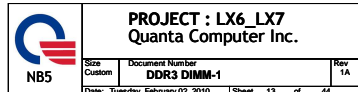
2,3,7,8,9,10,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41
+5V
+1.05V_VTT
+1.05V_VTT
+1.8V
+3V
+3VSS
+5V
+5VSS
+RTC_CELL



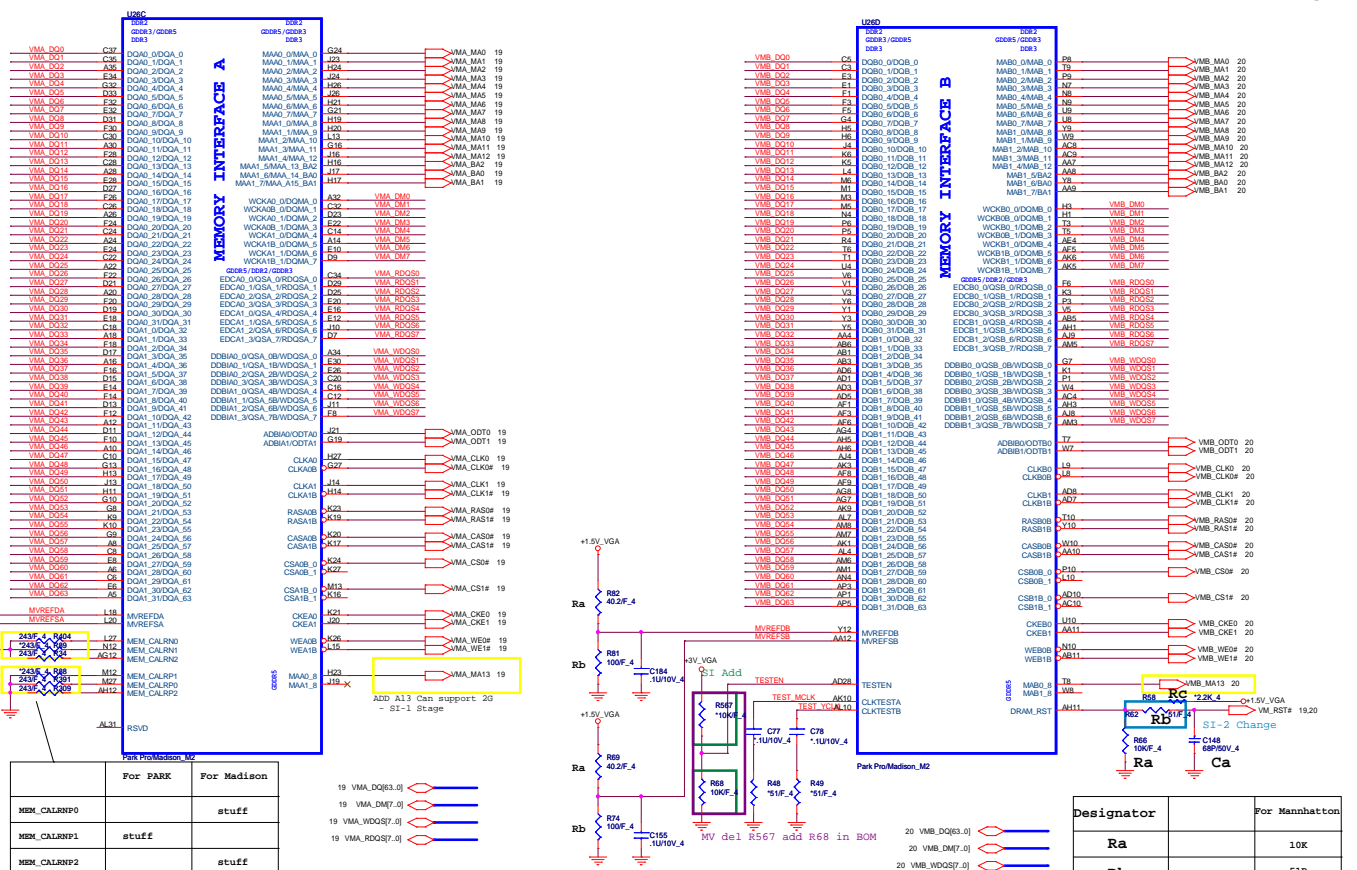
PROJECT : LX6_LX7
Quanta Computer Inc.

Size Custom	Document Number PCH 5/5 (POWER)	Rev 1A
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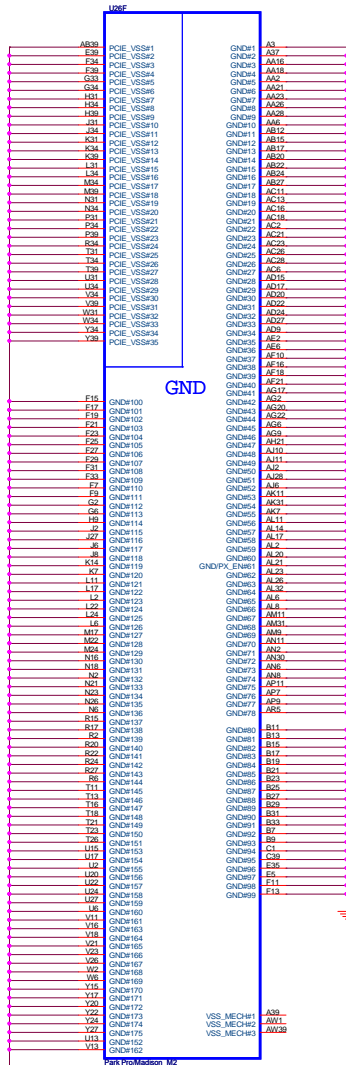












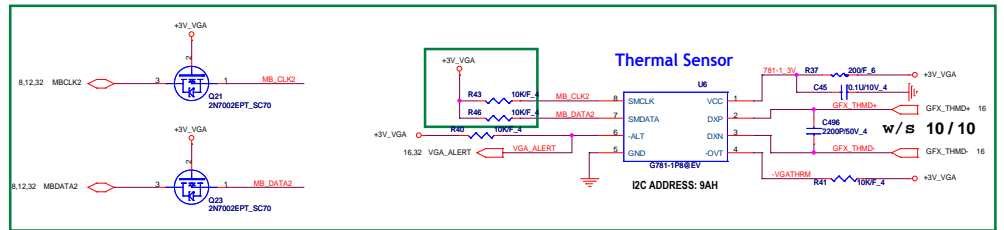
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: 50% Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1: Advertises the PCI-E device as 3.0 GT/s capable at power-on. 1: Tx de-emphasis enabled (Default setting for Desktop)	0
RSVD BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIOS_ROM_EN	GPIO22 ROMIDCFG2	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(9)	GPIO13(11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERIC HSYNC VSYNC	AUD[1] AUD[0] 0: No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	0 0 11

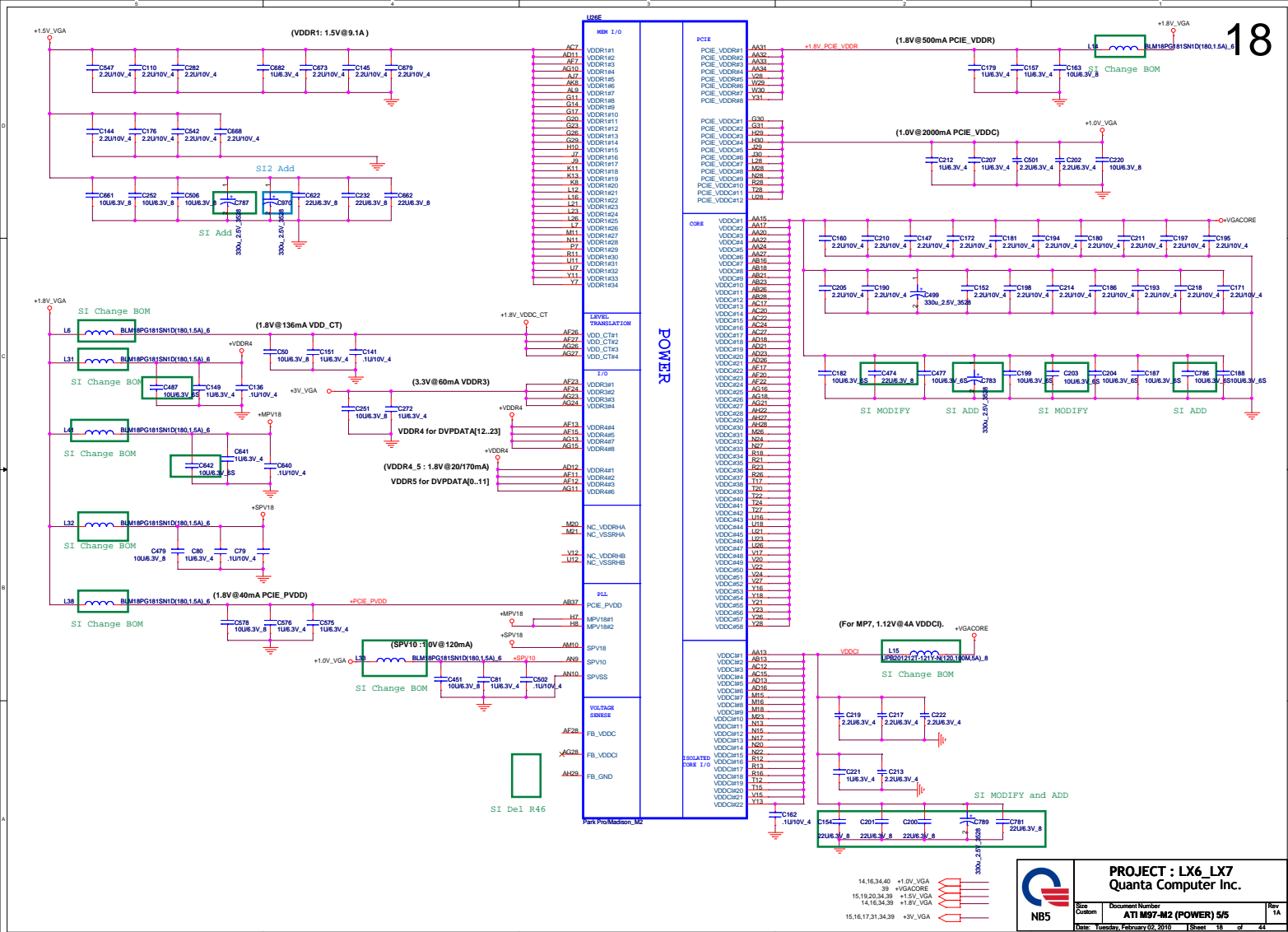
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: 50% Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1: Advertises the PCI-E device as 3.0 GT/s capable at power-on. 1: Tx de-emphasis enabled (Default setting for Desktop)	0
RSVD BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIOS_ROM_EN	GPIO22 ROMIDCFG2	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(9)	GPIO13(11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERIC HSYNC VSYNC	AUD[1] AUD[0] 0: No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	0 0 11

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: 50% Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1: Advertises the PCI-E device as 3.0 GT/s capable at power-on. 1: Tx de-emphasis enabled (Default setting for Desktop)	0
RSVD BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIOS_ROM_EN	GPIO22 ROMIDCFG2	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG2(9)	GPIO13(11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERIC HSYNC VSYNC	AUD[1] AUD[0] 0: No audio function 1: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	0 0 11

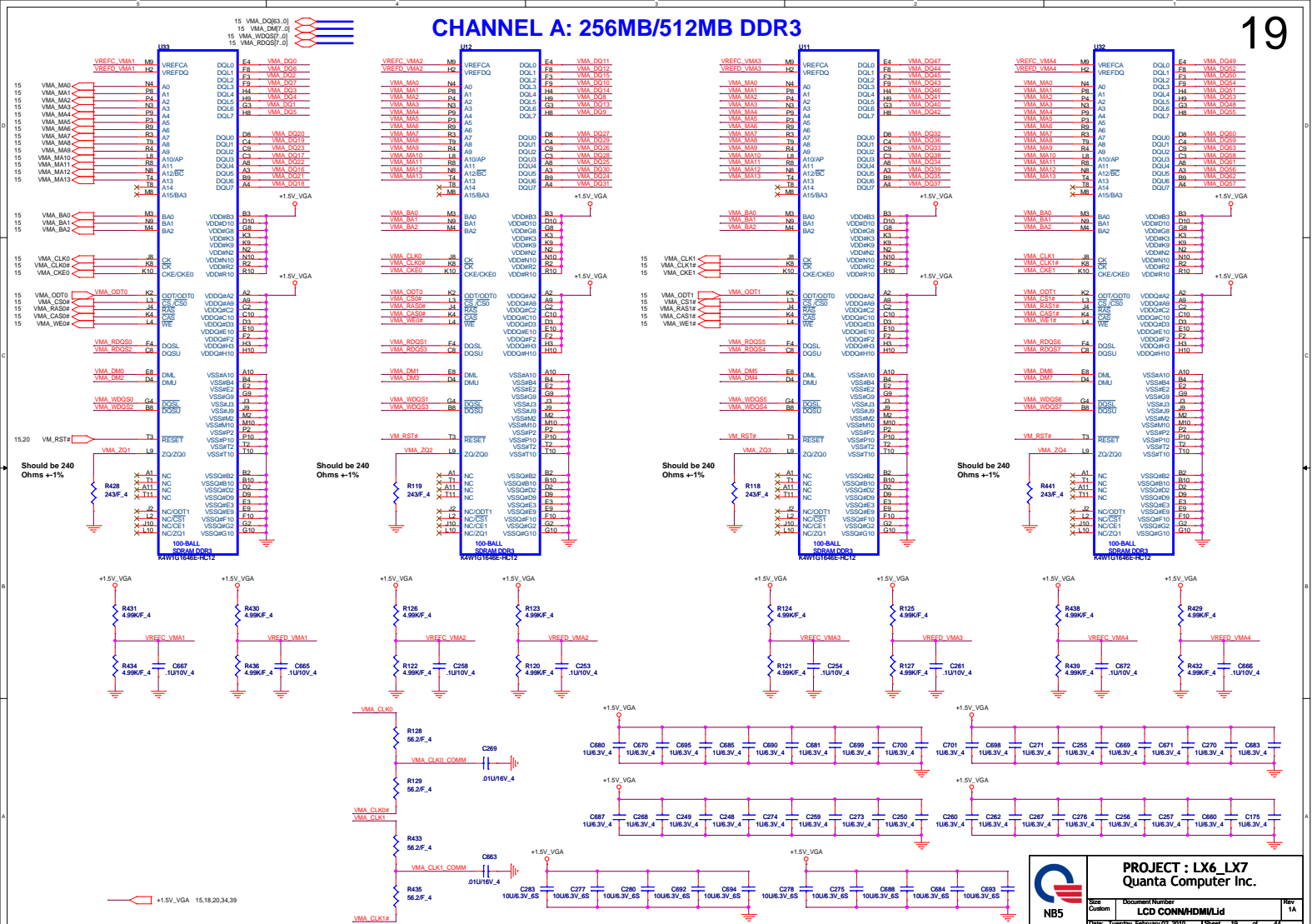
GPIO21_BB_EN

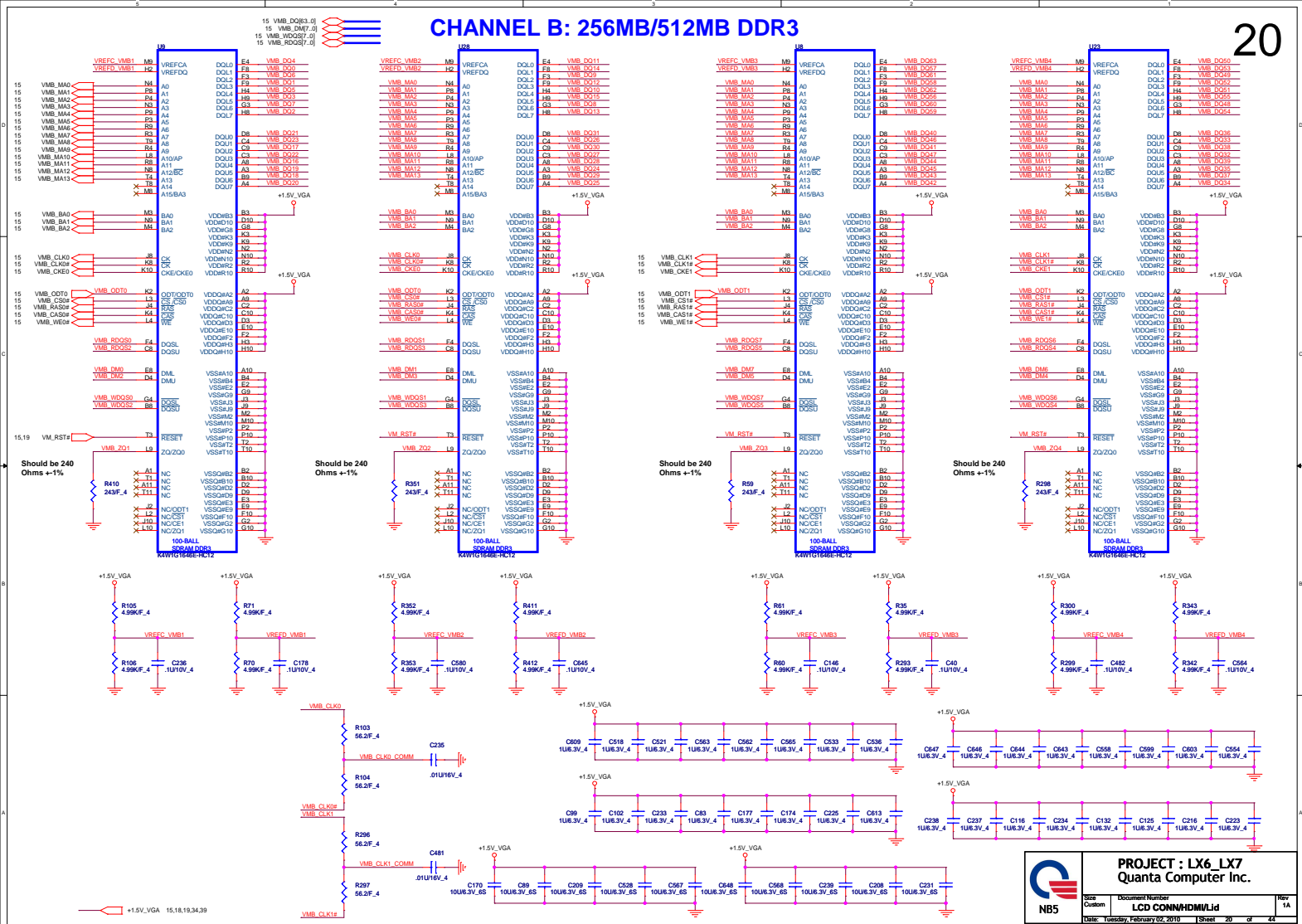
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

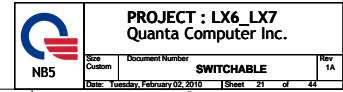


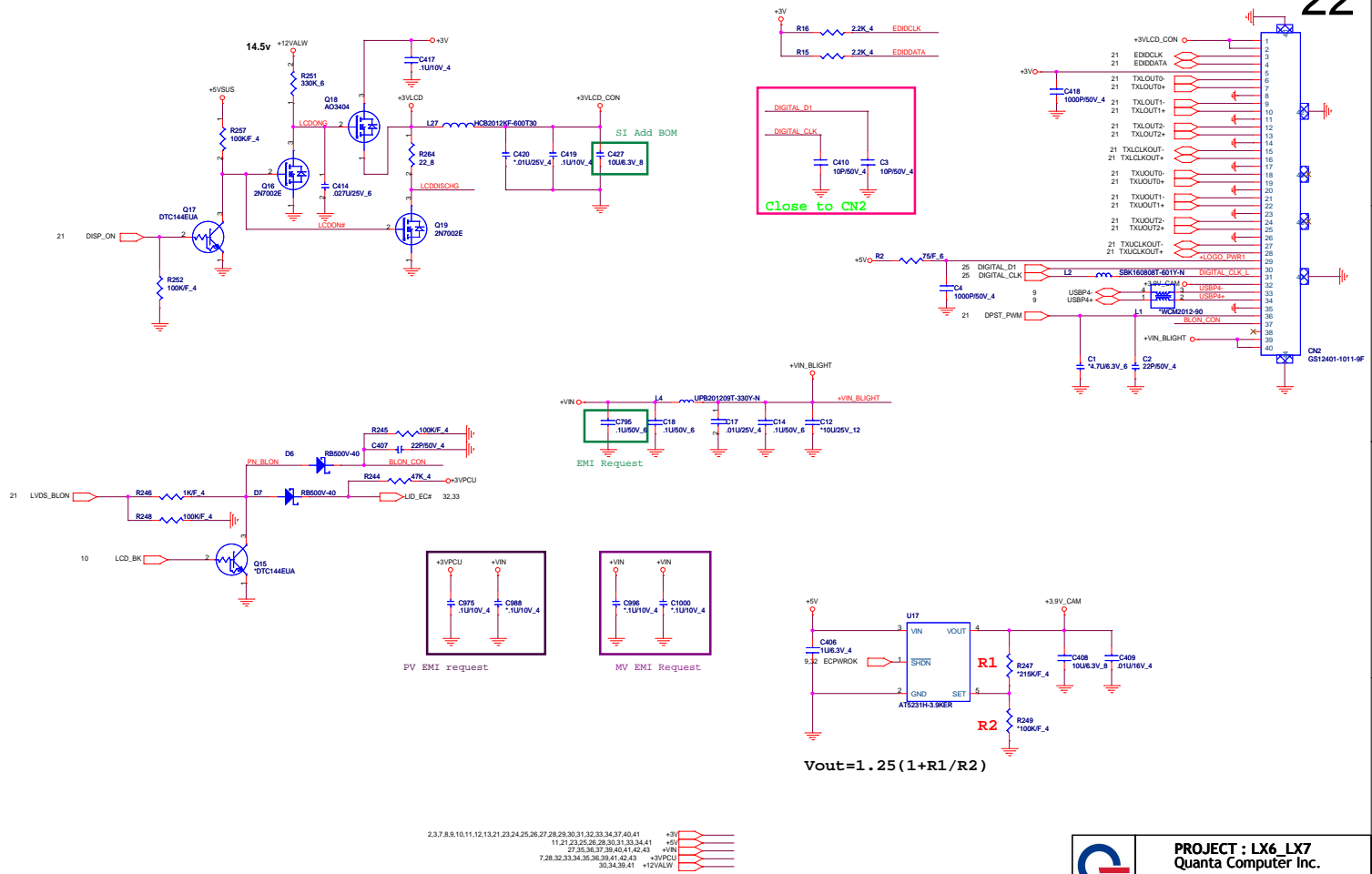


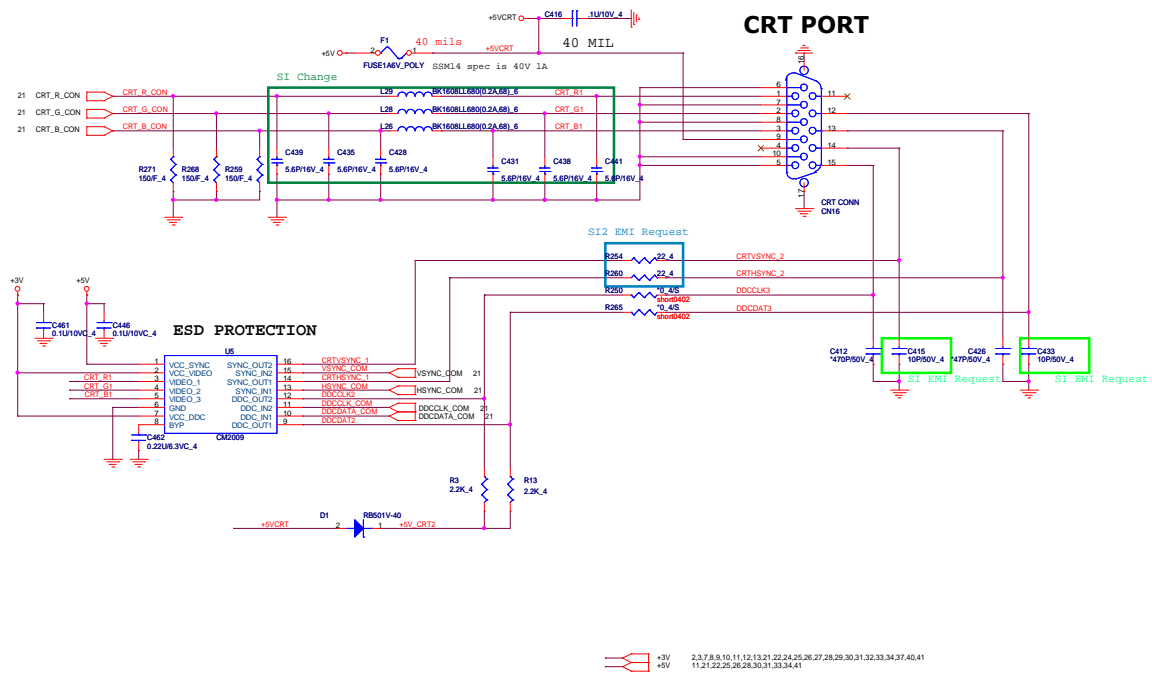
CHANNEL A: 256MB/512MB DDR3






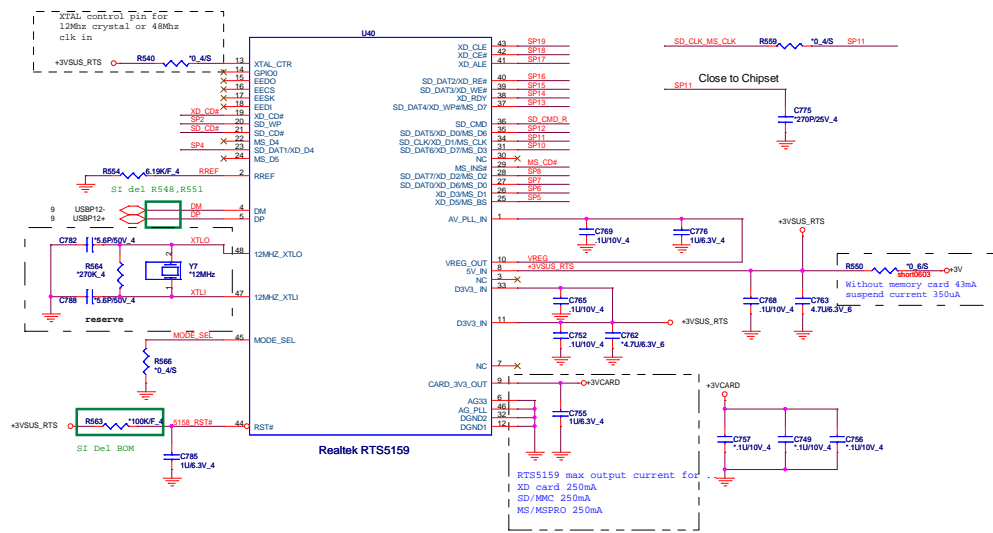




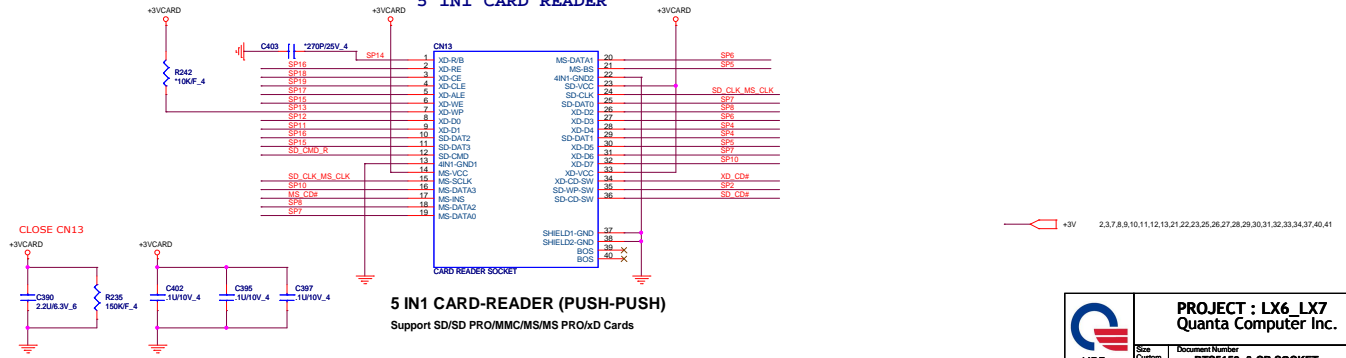


+3V 2,3,7,8,9,10,11,12,13,21,22,24,25,26,27,28,29,30,31,32,33,34,37,40,41
+5V 11,21,22,25,26,28,30,31,33,34,41

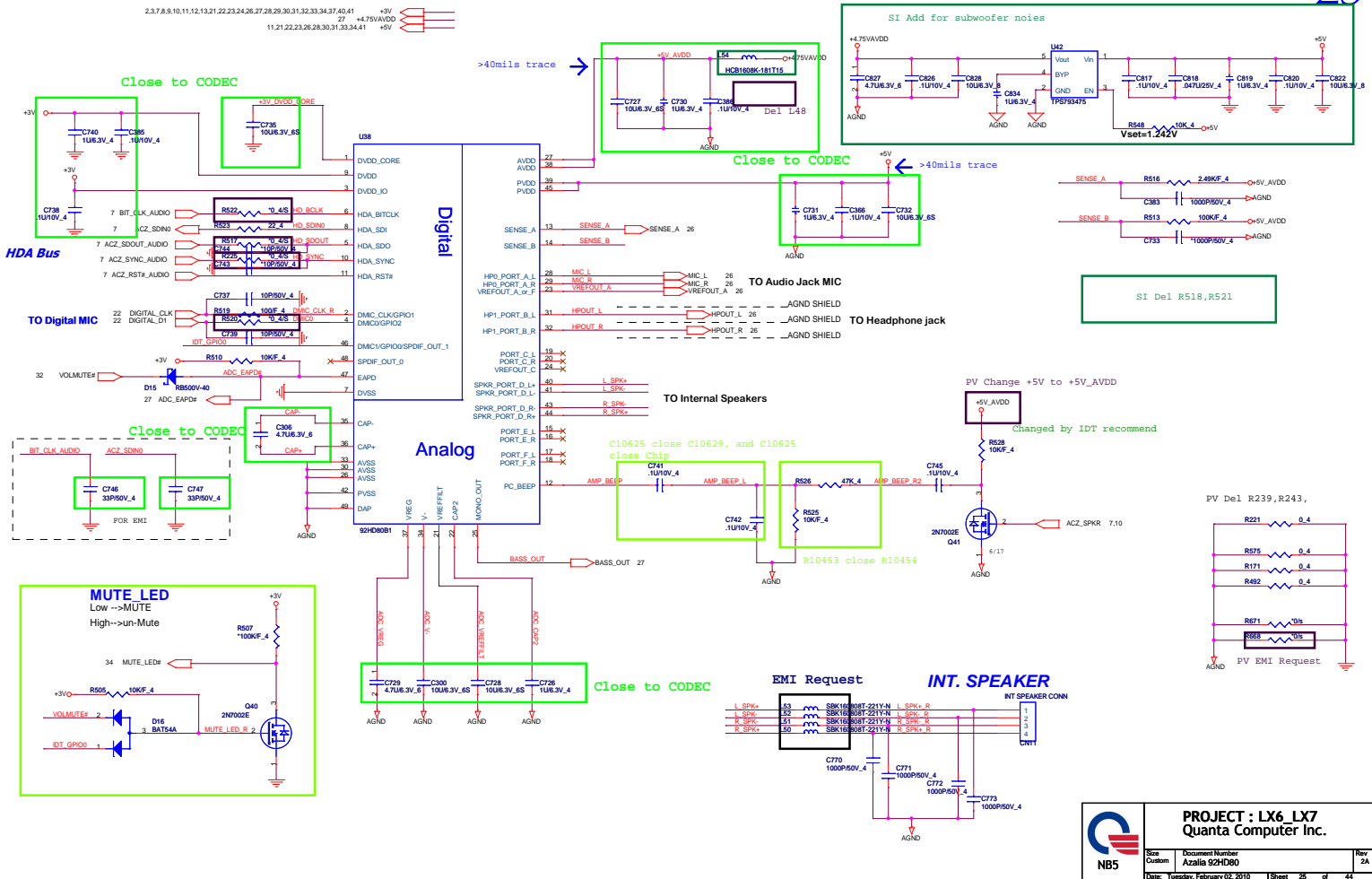
	PROJECT : LX6_LX7 Quanta Computer Inc.		
	Set Content	Document Number CRT/HDMI Conn	Rev 1A
	Date: Tuesday, February 03, 2010	Sheet: 23	of: 44



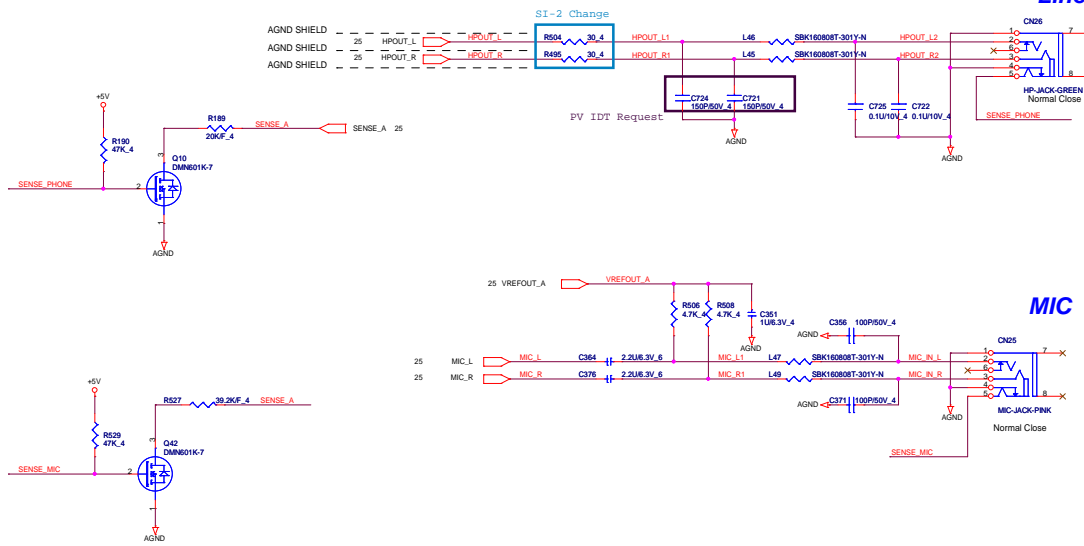
XD, MMC/SD, MS/MSP 5 IN1 CARD READER



NB5	PROJECT : LX6_LX7 Quanta Computer Inc.		
	Doc Number	Rev	1A
Doc	RT55159 & CR SOCKET	Rev	1A
Date	Tuesday, February 12, 2010	Sheet	31 of 44

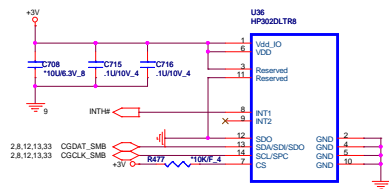


Line out




Accelerometer Sensor

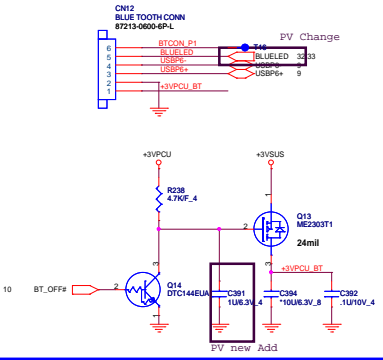
SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



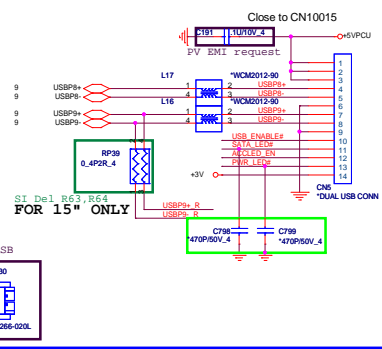
Pin 12: Low	38hex
Pin 12: unconnected/floating	3Ahex

 NB5	PROJECT : LX6_LX7 Quanta Computer Inc.	
	Size Custom	Document Number Audio Jack/Accelerometer
Date: Tuesday, February 02, 2010		Sheet 26 of 44

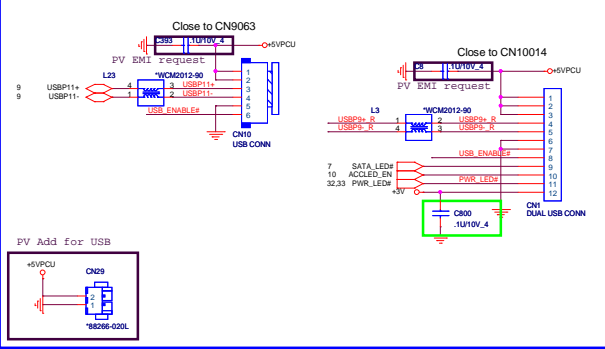
BLUETOOTH



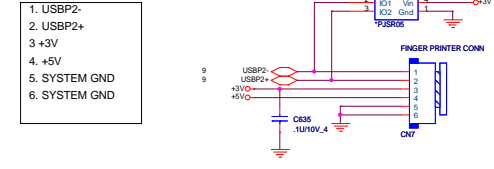
RIGHT SIDE USB2 for 17"



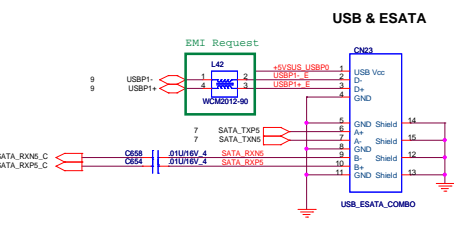
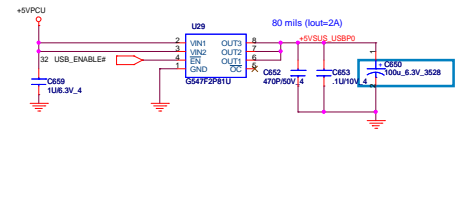
RIGHT SIDE USB for 15"



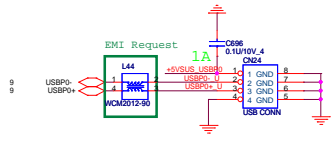
USB fingerprint CON



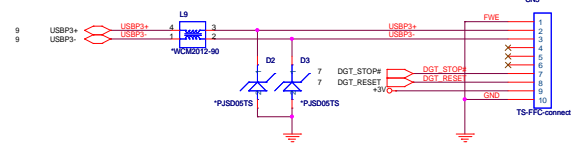
E-SATA



LEFT USB PORT



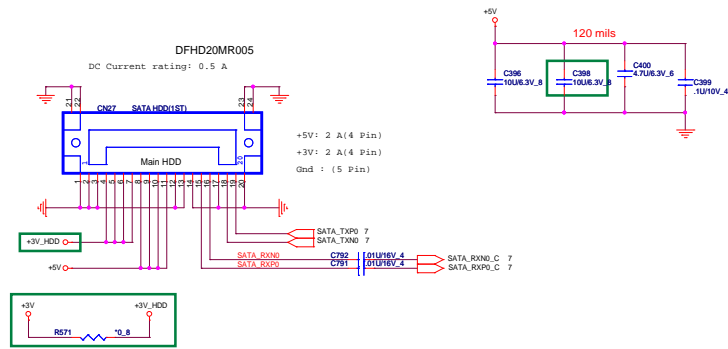
Touch screen for 15"



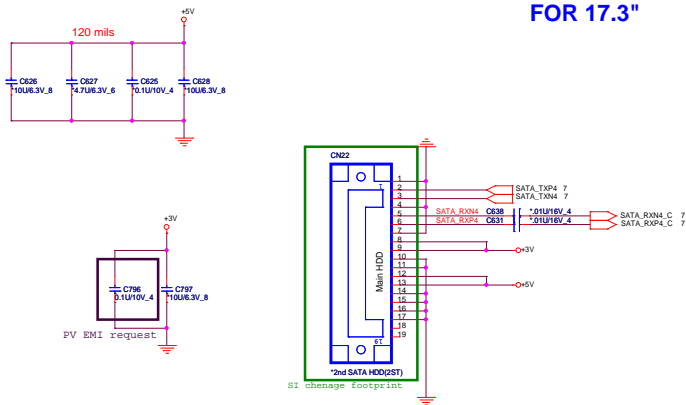
PROJECT : LX6_LX7
Quanta Computer Inc.

Rev	Document Number	Rev
1A	BT/WC/FT/Touchscreen	1A
	Date: Tuesday, February 03, 2010	Sheet 28 of 44

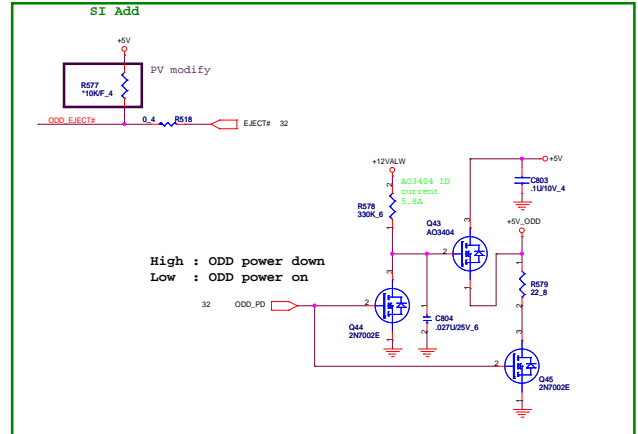
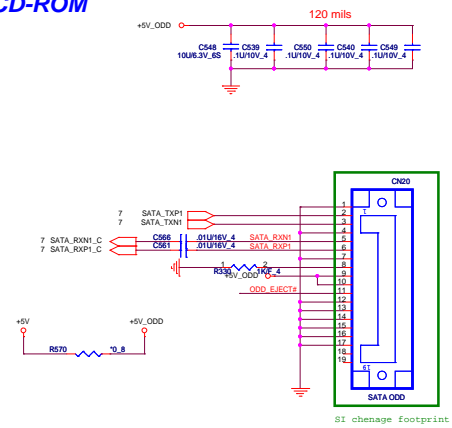
SATA HDD CONNECTOR



SATA_2 CONNECTOR FOR 17.3"

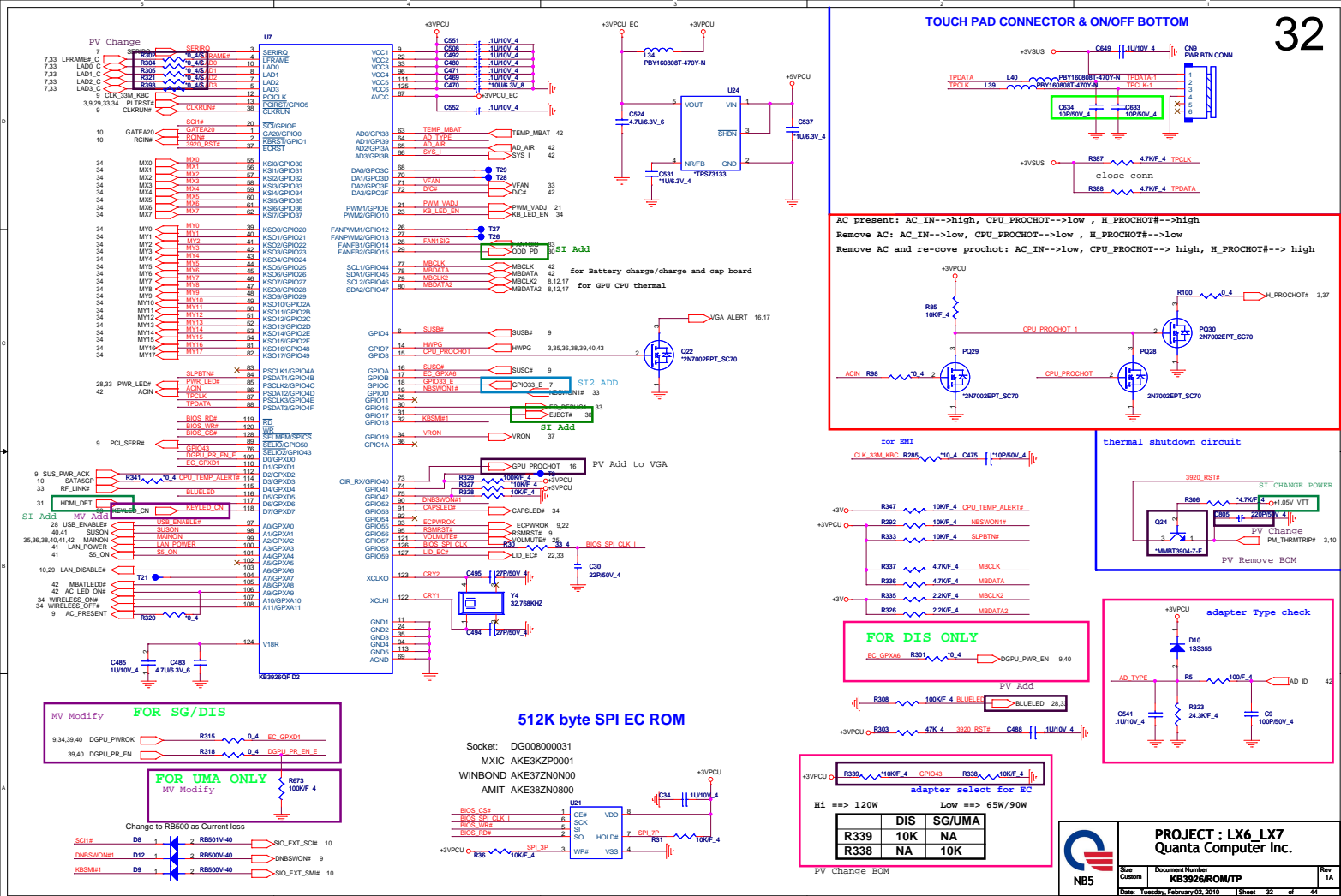


SATA CD-ROM

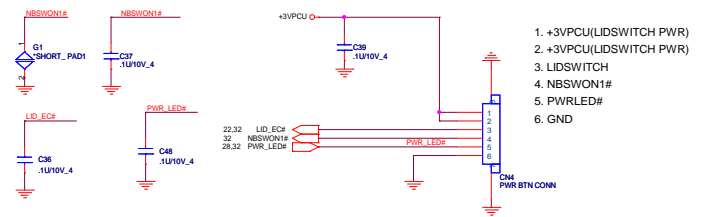


+3V	2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,31,32,33,34,37,40,41
+5V	11,21,22,23,25,26,28,31,33,34,41
+12VALW	22,34,39,41

PROJECT : LX6_LX7 Quanta Computer Inc.			
NB5	Set	Document Number	Rev
	ODD/HDD/ANT		1A
Date: Tuesday, February 15, 2010 Sheet 30 of 44			



POWER BOTTON CONNECT



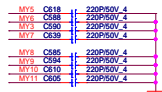
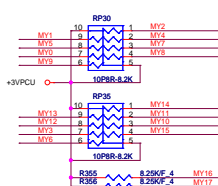
1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. NBSWON1#
5. PWRLED#
6. GND



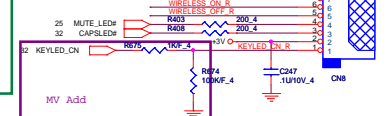
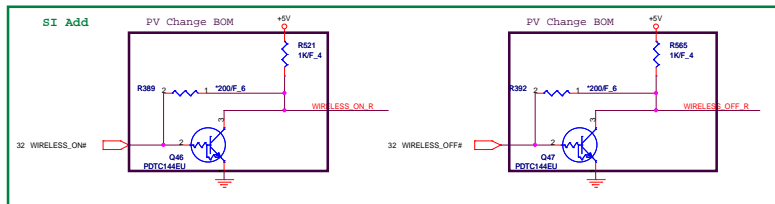
PROJECT : LX6_LX7
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN/FAN	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 33 of 44	

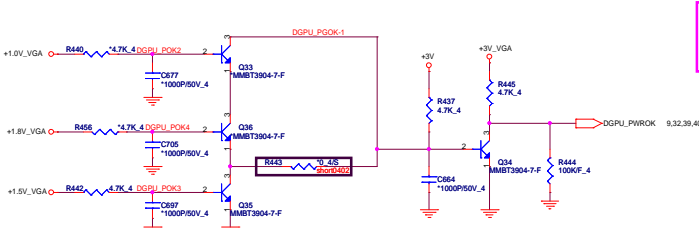
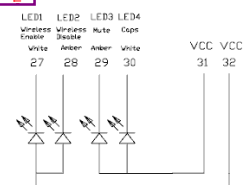
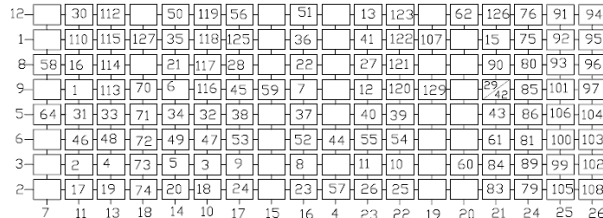
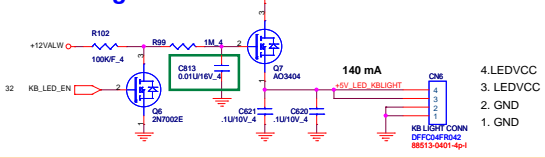
KEYBOARD PULL-UP



clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)



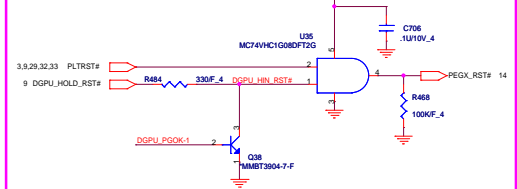
KB backlight for 15"



FOR DIS ONLY

PLTRST# R551 0.4 PEGX_RST#

FOR SG ONLY

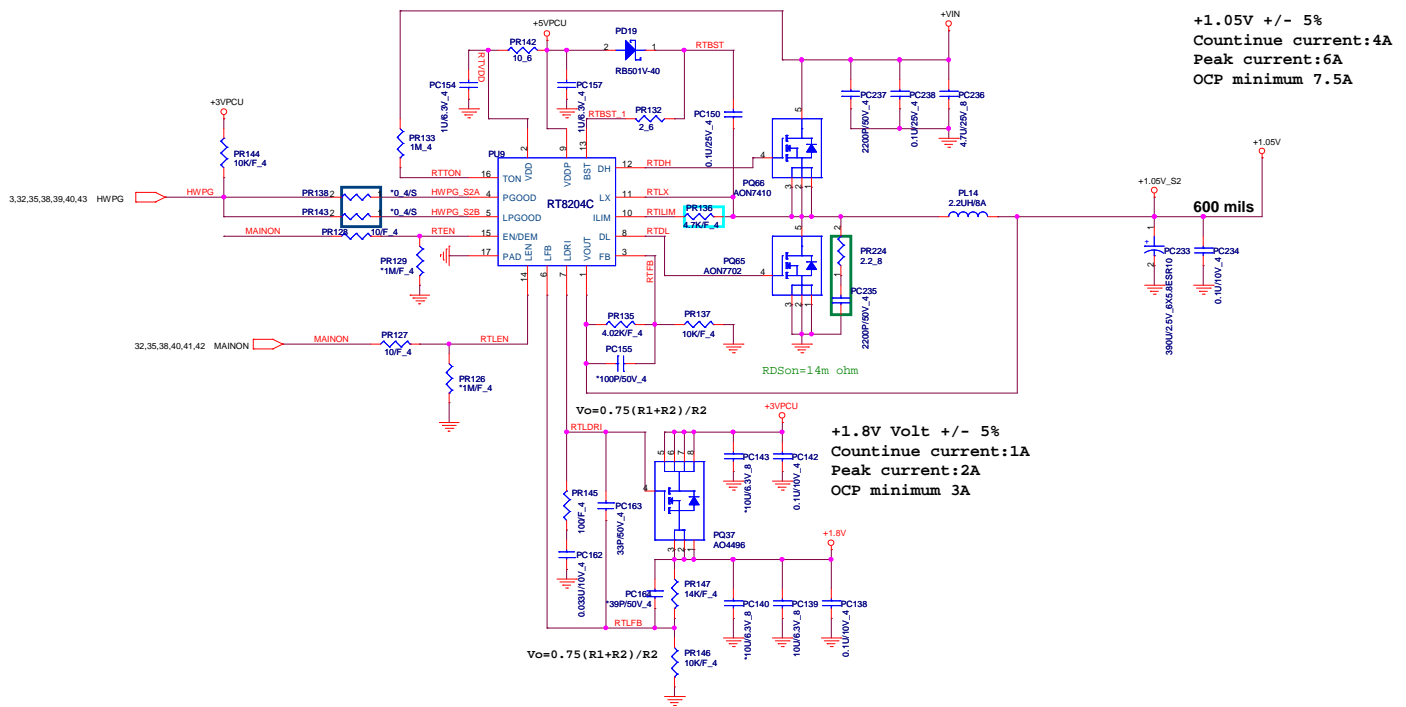


+3V	2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,41
+5V	11,21,22,23,24,25,26,27,28,29,30,31,32,33,41
+3VPCU	7,22,28,32,33,35,36,39,41,42,43
+5V_VGA	15,16,17,18,31,39
+12V_ALW	22,30,39,41
+1.0V_VGA	14,16,18,40
+1.5V_VGA	15,16,19,20,39
+1.8V_VGA	14,16,18,39

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Rev	1A
Doc#	15010101
Doc#	15010101
Doc#	15010101





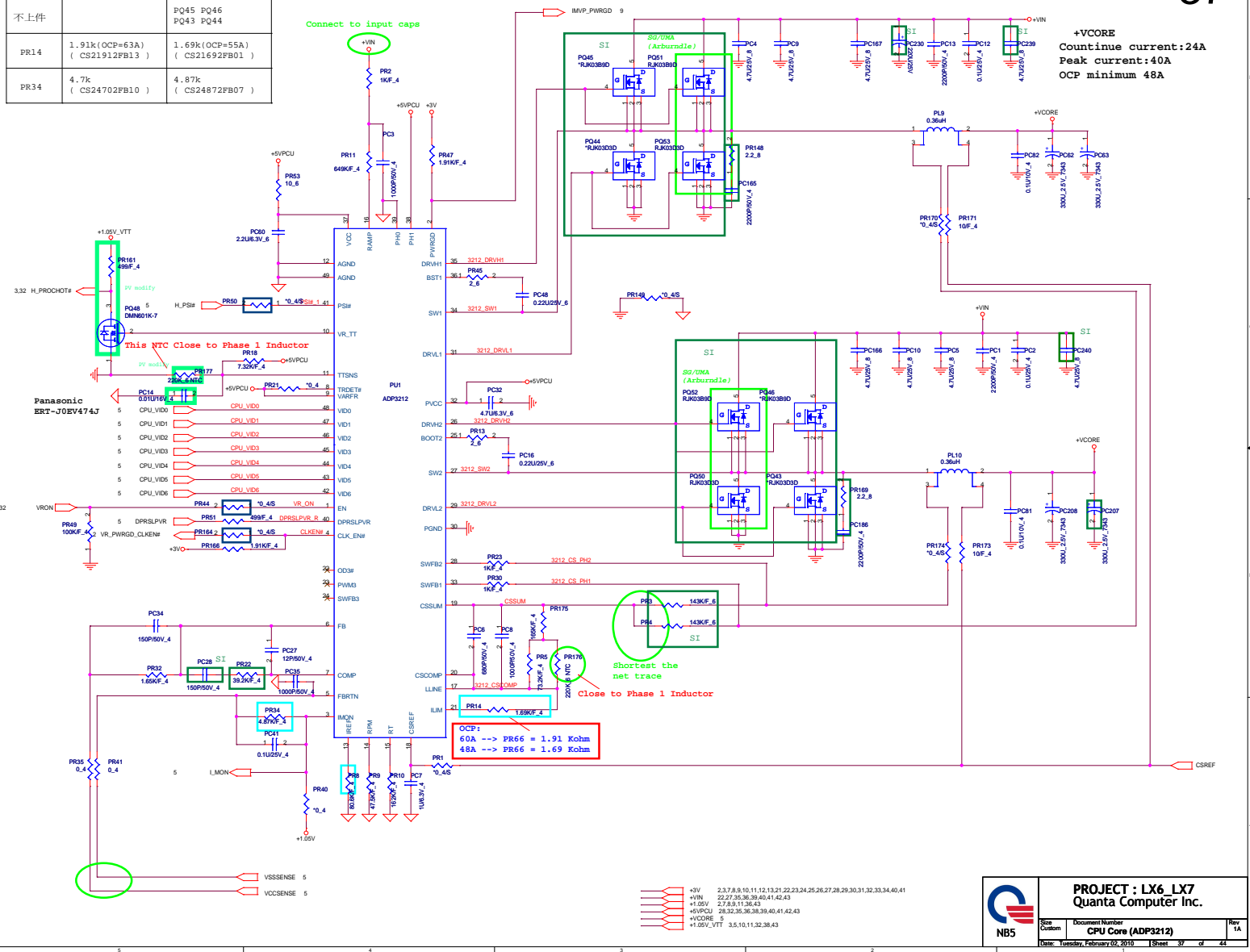
+1.8V	5,10,11,21,41
+VIN	22,27,35,37,39,40,41,42,43
+1.05V	2,7,8,9,11,37,43
+3VPCU	7,22,28,32,33,34,35,39,41,42,43
+5VPCU	28,32,35,37,38,39,40,41,42,43



PROJECT : LX6_LX7
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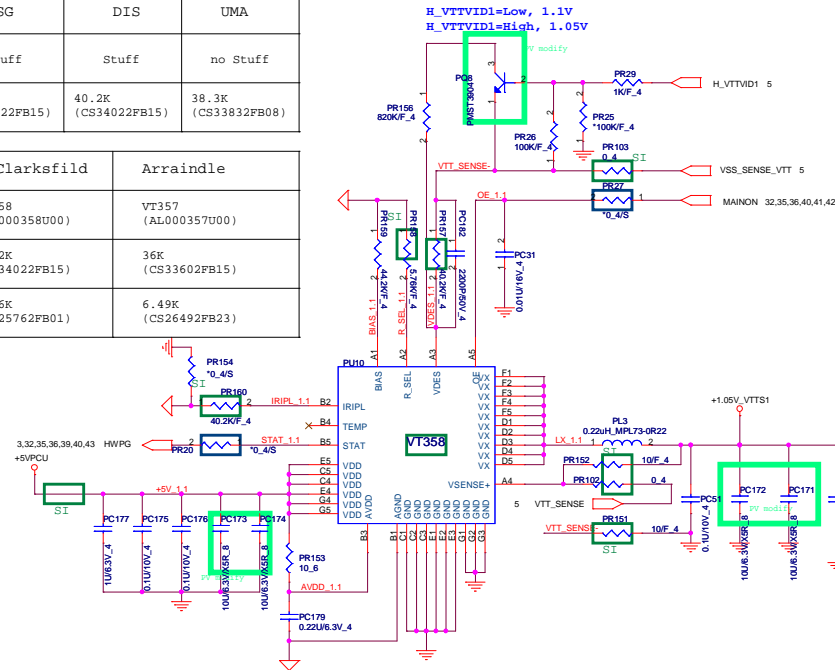
Size	Document Number	Rev
Custom	+1.05V/+1.8V (RT8204C)	1A
Date: Tuesday, February 02, 2010	Sheet 36 of 44	

	DIS (Clarksfield)	SG/UMA (Arbunrdle)
不上件		PQ45 PQ46 PQ43 PQ44
PR14	1.91k (OCP=63A) (CS21912FB13)	1.69k (OCP=55A) (CS21692FB01)
PR34	4.7k (CS24702FB10)	4.87k (CS24872FB07)



	SG	DIS	UMA
PR156 PR26 PR29 PQ8	Stuff	Stuff	no Stuff
PR157	40.2K (CS34022FB15)	40.2K (CS34022FB15)	38.3K (CS33832FB08)

	Clarksfield	Arrairdle
PU10	VT358 (AL000358U00)	VT357 (AL000357U00)
PR160	40.2K (CS34022FB15)	36K (CS33602FB15)
PR158	5.76K (CS25762FB01)	6.49K (CS26492FB23)

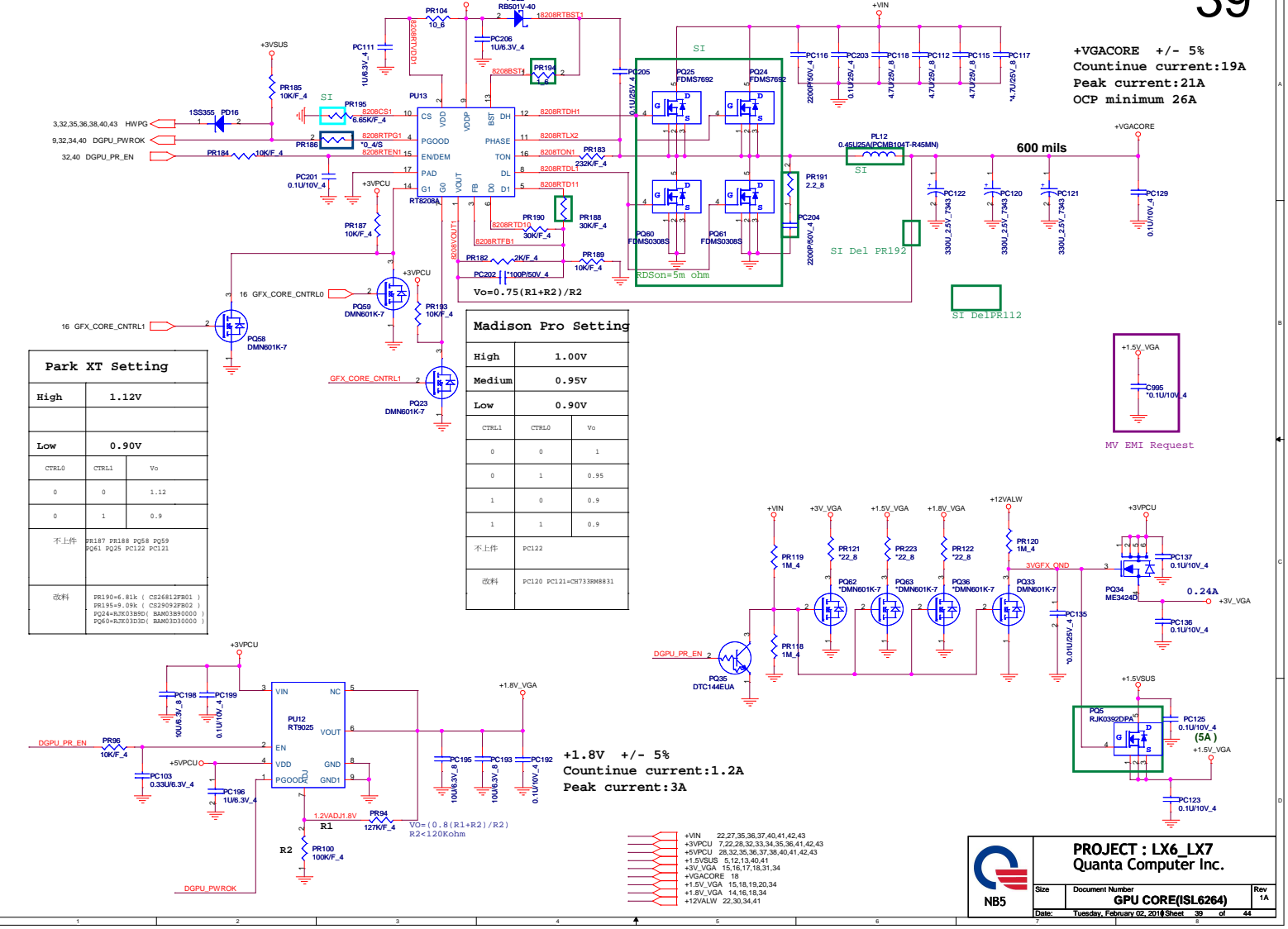


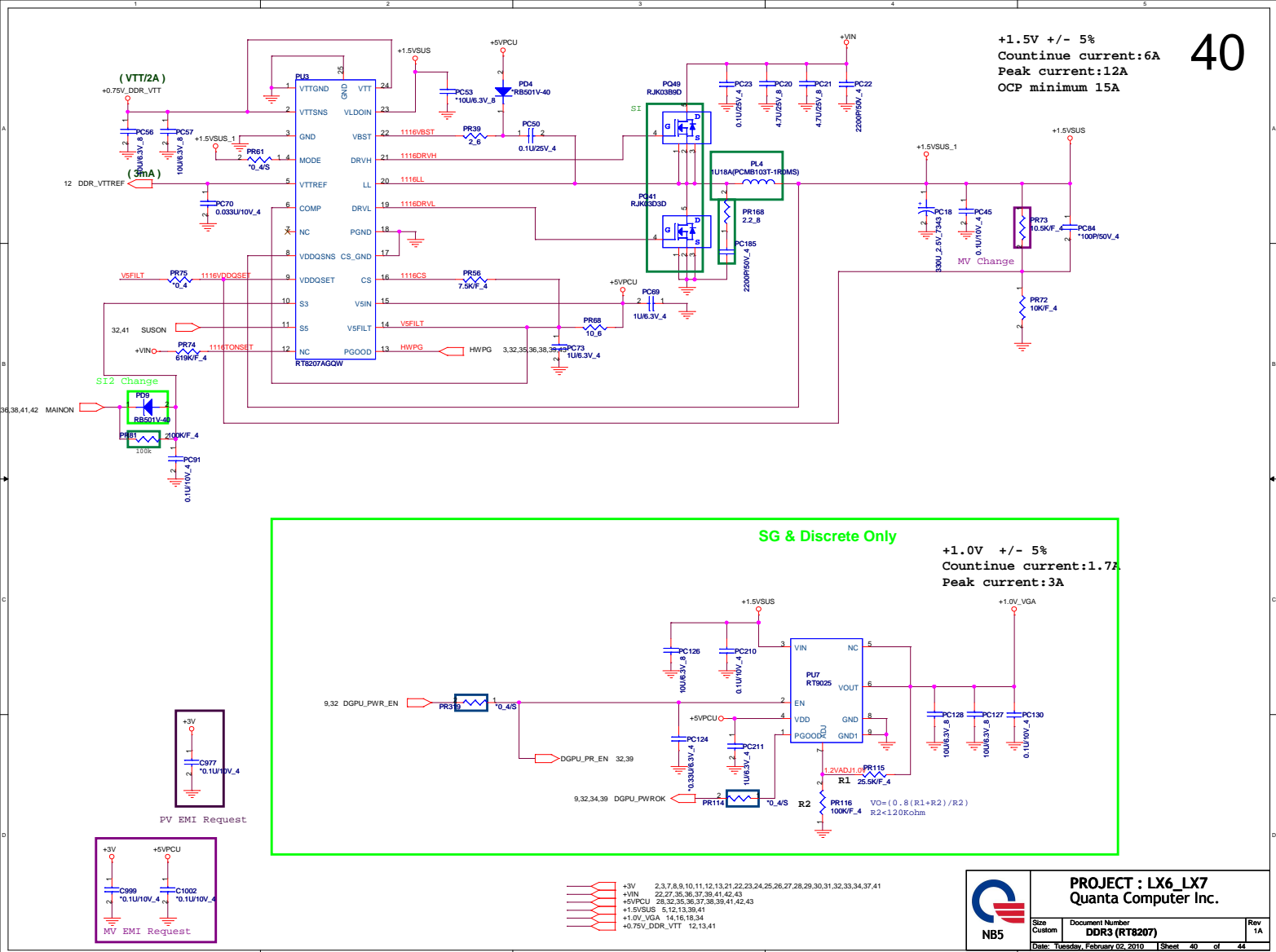
+1.05V_VTT +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



PROJECT : LX6_LX7
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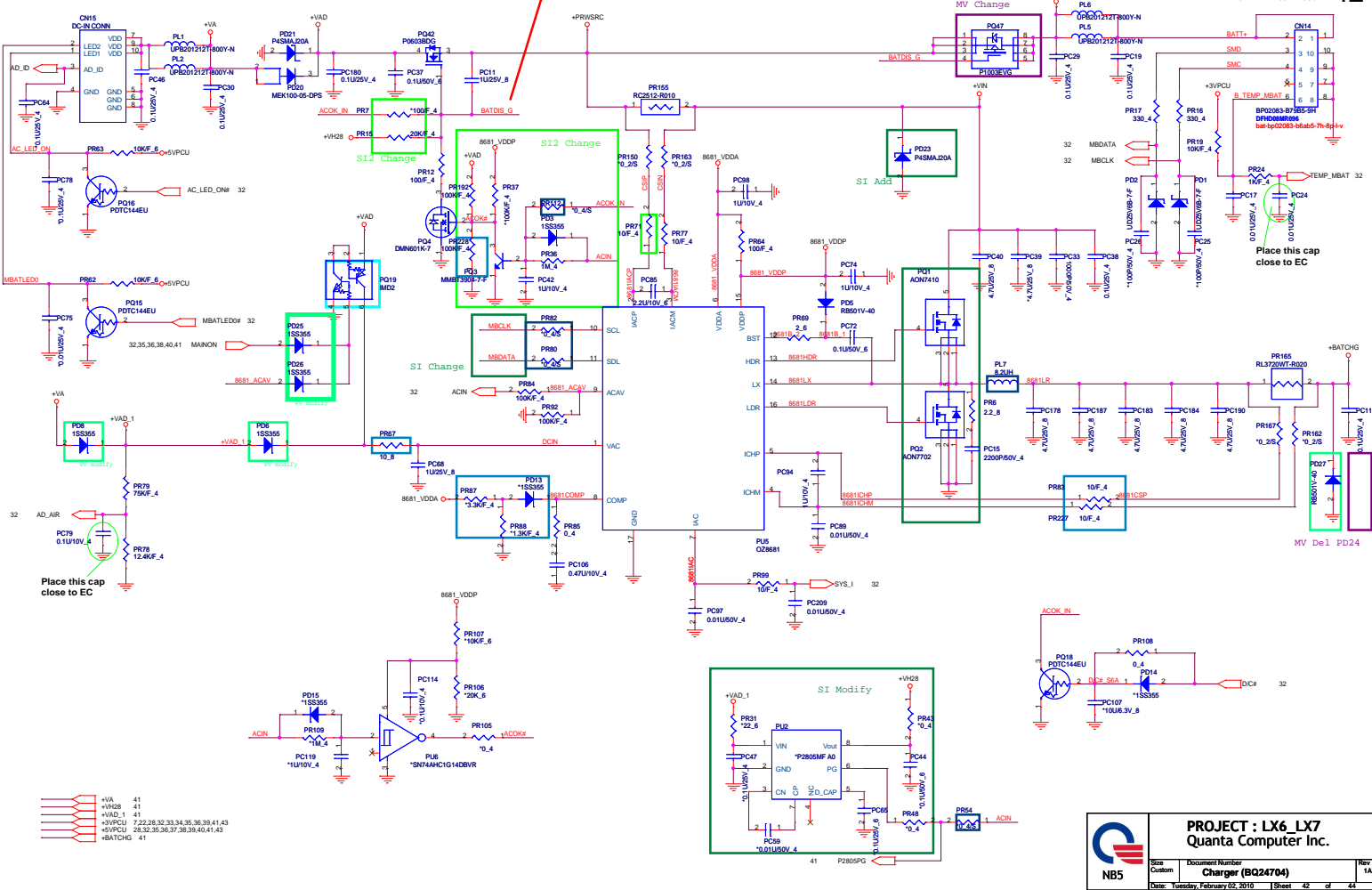
Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	1A
Date: Tuesday, February 02, 2010	Sheet 38 of 44	

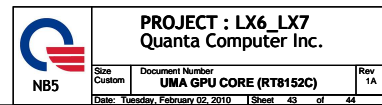


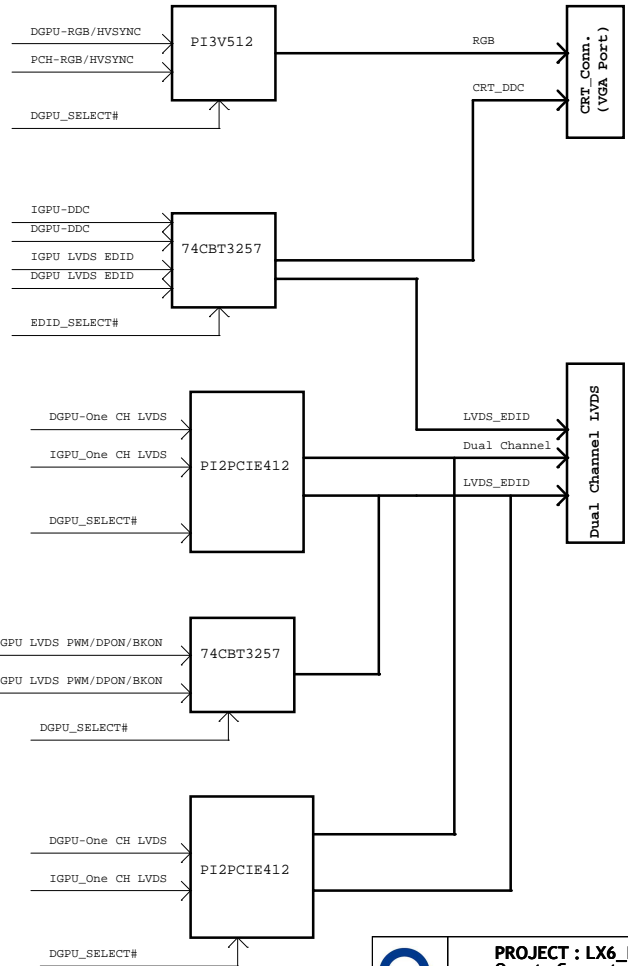
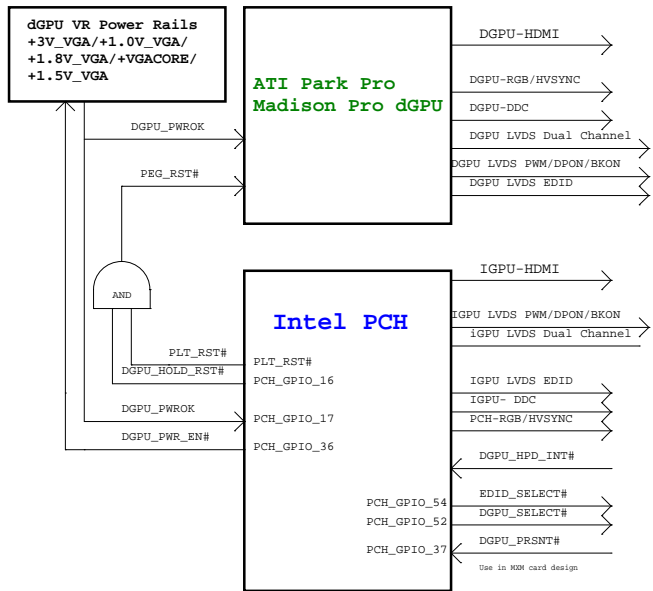





Do Not add test pad on BATDIS_G signal







Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO16	DGPU_HOLD_RST#
PCH_GPIO36	DGPU_PWR_EN#
PCH_GPIO17	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO37	DGPU_PRNT#



PROJECT : LX6 LX7

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Size	Document Number	Rev
Custom	Switch Blockdiagram	1A
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